

### OVERVIEW

The CF5073 series are VCXO ICs with built-in varicap diode. They use a recently developed negative-resistance switching oscillation circuit, at oscillation startup and during normal oscillation, for both good oscillation startup characteristics and wide pullrange. Furthermore, it employs a CMOS process varicap diode, and also features all the necessary VCXO structure circuit components on a single chip, forming a VCXO module with just the connection of an external crystal.

### FEATURES

- 3.0 to 3.6V supply voltage range
- 10MHz to 60MHz operating frequency (varies with version)
- Uses negative-resistance switching function
- Varicap diode built-in
- Frequency divider built-in (varies with version:  $f_O$ ,  $f_O/2$ ,  $f_O/4$ ,  $f_O/8$ ,  $f_O/16$ ,  $f_O/32$ )
- CMOS output level
- $50 \pm 10\%$  output duty
- 6mA (min) output drive capability
- 15pF output load capacitance  $C_L$
- Standby function (high impedance in standby mode)
- Chip form (CF5073××)

### SERIES LINEUP

Version	Typical oscillation frequency <sup>1</sup> [MHz]	Output frequency					
		CF5073×1	CF5073×2 <sup>2</sup>	CF5073×3 <sup>2</sup>	CF5073×4 <sup>2</sup>	CF5073×5 <sup>2</sup>	CF5073×6 <sup>2</sup>
CF5073A×	16	$f_O$	$f_O/2$	$f_O/4$	$f_O/8$	$f_O/16$	$f_O/32$
CF5073B×	23						
CF5073C×	30						
CF5073D×	37						
CF5073E×	44						
CF5073F×	51						

- The typical oscillation frequency is the oscillation frequency criteria for use when selecting the device version. Note that the oscillation characteristics and pullability vary with the crystal used and the mounting conditions. Even for the same frequency, the optimal version can vary with crystal characteristics, so careful evaluation should be exercised when selecting the device version.
- These versions are produced after receiving a purchase order. Please ask our Sales & Marketing section for further detail.

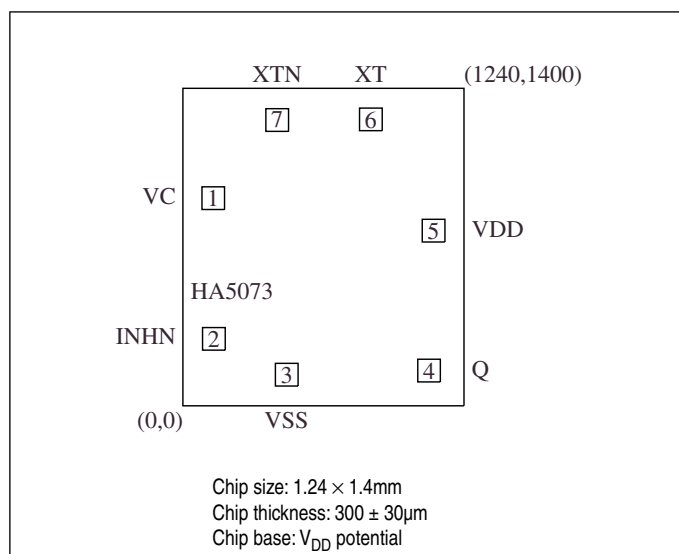
### APPLICATIONS

- VCXO modules
- Communications application
- Networking application
- Broadcasting application

### ORDERING INFORMATION

Device	Package
CF5073××-1	Chip form

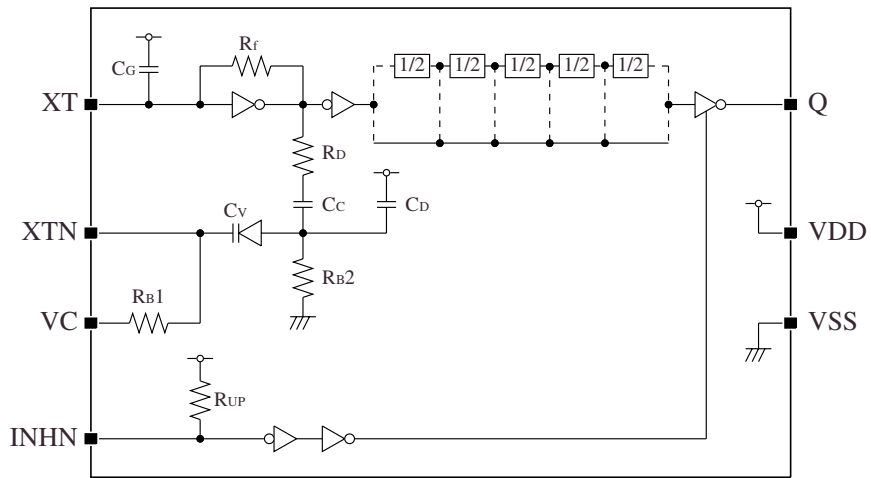
## PAD LAYOUT

(Unit:  $\mu\text{m}$ )

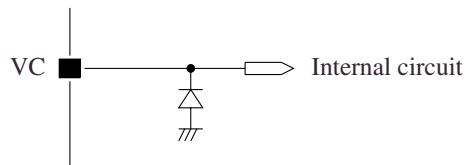
## PAD DESCRIPTION AND DIMENSIONS

Pad No.	Name	I/O	Description	Function	Pad dimensions [ $\mu\text{m}$ ]	
					X	Y
1	VC	I	Oscillation frequency control voltage input pin	Positive polarity (frequency increases with increasing voltage)	134	915
2	INH	I	Output state control voltage input pin	High-impedance output when LOW, pull-up resistor built-in	137	295
3	VSS	-	(-) supply pin		458	137
4	Q	O	Output pin	Output frequency determined by internal circuit to one of $f_O, f_O/2, f_O/4, f_O/8, f_O/16, f_O/32$	1086	155
5	VDD	-	(+) supply pin		1106	772
6	XT	I	Amplifier input pin	Crystal connection pins. Crystal is connected between XT and XTN.	829	1263
7	XTN	O	Amplifier output pin		416	1260

**BLOCK DIAGRAM**



Note. ESD of XT pin is inferior to other pins.  
 ESD of all pins excluding XT pin is equivalent to that of our other oscillator products.  
 VC pin has no protection circuit at V<sub>DD</sub> side. (See figure below.)



**ABSOLUTE MAXIMUM RATINGS**

$V_{SS} = 0V$  unless otherwise noted.

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage range	$V_{DD}$		-0.5 to 7.0	V
Input voltage range	$V_{IN}$	All input pins excluding VC pin	-0.5 to $V_{DD} + 0.5$	V
		VC pin	-0.5 to $V_{DD} + 2.5^1$	V
Output voltage range	$V_{OUT}$		-0.5 to $V_{DD} + 0.5$	V
Operating temperature range	$T_{opr}$		-40 to +85	°C
Storage temperature range	$T_{STG}$		-65 to +150	°C
Output current	$I_{OUT}$		20	mA

1. It should not exceed +7.0V.

**RECOMMENDED OPERATING CONDITIONS**

$V_{SS} = 0V$ ,  $f = 10MHz$  to  $60MHz$ ,  $C_L \leq 15pF$  unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
Operating supply voltage	$V_{DD}$		3.0	-	3.6	V
Input voltage	$V_{IN}$		$V_{SS}$	-	$V_{DD}$	V
Operating temperature	$T_{OPR}$		-40	-	+85	°C

## ELECTRICAL CHARACTERISTICS

CF5073A $\times$ 

$V_{DD} = 3.0$  to  $3.6V$ ,  $V_C = 1.65V$ ,  $V_{SS} = 0V$ ,  $T_a = -40$  to  $+85^\circ C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit	
			Min	Typ	Max		
HIGH-level output voltage	$V_{OH}$	Q: Measurement circuit 1, $I_{OH} = 6mA$	2.5	2.75	–	V	
LOW-level output voltage	$V_{OL}$	Q: Measurement circuit 1, $I_{OL} = 6mA$	–	0.2	0.4	V	
Output leakage current	$I_Z$	Q: Measurement circuit 6, INHN = LOW	$V_{OH} = V_{DD}$	–	–	10	$\mu A$
			$V_{OL} = V_{SS}$	–	–	10	$\mu A$
HIGH-level input voltage	$V_{IH}$	INHN	$0.7V_{DD}$	–	–	V	
LOW-level input voltage	$V_{IL}$	INHN	–	–	$0.3V_{DD}$	V	
Current consumption	$I_{DD}$	Measurement circuit 2, load circuit 1, INHN = open, $C_L = 15pF$ , $f = 16MHz$	CF5073A1	–	8	20	$mA$
			CF5073A2	–	7.5	19.5	$mA$
			CF5073A3	–	7	19.5	$mA$
			CF5073A4 to 6	–	7	19	$mA$
INHN pull-up resistance	$R_{UP}$	Measurement circuit 3	50	100	180	$k\Omega$	
Built-in resistance	$R_f$	Design value. A monitor pattern on a wafer is tested.	150	300	540	$k\Omega$	
	$R_D$		0.67	0.96	1.25	$k\Omega$	
	$R_{B1}$	Measurement circuit 4	100	200	360	$k\Omega$	
	$R_{B2}$	Design value. A monitor pattern on a wafer is tested.	50	100	180	$k\Omega$	
Built-in capacitance	$C_V$	Design value. A monitor pattern on a wafer is tested.	$V_C = 0.3V$	11.0	14.4	17.8	$pF$
			$V_C = 3.0V$	2.4	4.0	5.6	$pF$
	$C_G$	Design value. A monitor pattern on a wafer is tested.	25.5	30	34.5	$pF$	
	$C_D$		34	40	46	$pF$	
	$C_C$		8.5	10	11.5	$pF$	

**CF5073 series**

**CF5073B**×

$V_{DD} = 3.0$  to  $3.6V$ ,  $V_C = 1.65V$ ,  $V_{SS} = 0V$ ,  $T_a = -40$  to  $+85^\circ C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit	
			Min	Typ	Max		
HIGH-level output voltage	$V_{OH}$	Q: Measurement circuit 1, $I_{OH} = 6mA$	2.5	2.75	–	V	
LOW-level output voltage	$V_{OL}$	Q: Measurement circuit 1, $I_{OL} = 6mA$	–	0.2	0.4	V	
Output leakage current	$I_Z$	Q: Measurement circuit 6, INHN = LOW	$V_{OH} = V_{DD}$	–	–	10	$\mu A$
			$V_{OL} = V_{SS}$	–	–	10	$\mu A$
HIGH-level input voltage	$V_{IH}$	INHN	$0.7V_{DD}$	–	–	V	
LOW-level input voltage	$V_{IL}$	INHN	–	–	$0.3V_{DD}$	V	
Current consumption	$I_{DD}$	Measurement circuit 2, load circuit 1, INHN = open, $C_L = 15pF$ , $f = 23MHz$	CF5073B1	–	9	22	mA
			CF5073B2	–	8	21	mA
			CF5073B3	–	7.5	20.5	mA
			CF5073B4 to 6	–	7.5	20.5	mA
INHN pull-up resistance	$R_{UP}$	Measurement circuit 3	50	100	180	$k\Omega$	
Built-in resistance	$R_f$	Design value. A monitor pattern on a wafer is tested.	150	300	540	$k\Omega$	
	$R_D$		0.50	0.72	0.94	$k\Omega$	
	$R_{B1}$	Measurement circuit 4	100	200	360	$k\Omega$	
	$R_{B2}$	Design value. A monitor pattern on a wafer is tested.	50	100	180	$k\Omega$	
Built-in capacitance	$C_V$	Design value. A monitor pattern on a wafer is tested.	$V_C = 0.3V$	11.0	14.6	18.2	pF
			$V_C = 3.0V$	2.3	4.0	5.7	pF
	$C_G$	Design value. A monitor pattern on a wafer is tested.	25.5	30	34.5	pF	
	$C_D$		34	40	46	pF	
	$C_C$		12.7	15	17.3	pF	

**CF5073 series**

**CF5073C**×

$V_{DD} = 3.0$  to  $3.6V$ ,  $V_C = 1.65V$ ,  $V_{SS} = 0V$ ,  $T_a = -40$  to  $+85^\circ C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit	
			Min	Typ	Max		
HIGH-level output voltage	$V_{OH}$	Q: Measurement circuit 1, $I_{OH} = 6mA$	2.5	2.75	–	V	
LOW-level output voltage	$V_{OL}$	Q: Measurement circuit 1, $I_{OL} = 6mA$	–	0.2	0.4	V	
Output leakage current	$I_Z$	Q: Measurement circuit 6, INHN = LOW	$V_{OH} = V_{DD}$	–	–	10	$\mu A$
			$V_{OL} = V_{SS}$	–	–	10	$\mu A$
HIGH-level input voltage	$V_{IH}$	INHN	$0.7V_{DD}$	–	–	V	
LOW-level input voltage	$V_{IL}$	INHN	–	–	$0.3V_{DD}$	V	
Current consumption	$I_{DD}$	Measurement circuit 2, load circuit 1, INHN = open, $C_L = 15pF$ , $f = 30MHz$	CF5073C1	–	10	24	$mA$
			CF5073C2	–	9	23	$mA$
			CF5073C3	–	8.5	22.5	$mA$
			CF5073C4 to 6	–	8	22	$mA$
INHN pull-up resistance	$R_{UP}$	Measurement circuit 3	50	100	180	$k\Omega$	
Built-in resistance	$R_f$	Design value. A monitor pattern on a wafer is tested.	150	300	540	$k\Omega$	
	$R_D$		0.50	0.72	0.94	$k\Omega$	
	$R_{B1}$	Measurement circuit 4	100	200	360	$k\Omega$	
	$R_{B2}$	Design value. A monitor pattern on a wafer is tested.	50	100	180	$k\Omega$	
Built-in capacitance	$C_V$	Design value. A monitor pattern on a wafer is tested.	$V_C = 0.3V$	11.0	14.6	18.2	$pF$
			$V_C = 3.0V$	2.3	4.0	5.7	$pF$
	$C_G$	Design value. A monitor pattern on a wafer is tested.	25.5	30	34.5	$pF$	
	$C_D$		25.5	30	34.5	$pF$	
	$C_C$		29.7	35	40.3	$pF$	

**CF5073 series**

**CF5073D**×

$V_{DD} = 3.0$  to  $3.6V$ ,  $V_C = 1.65V$ ,  $V_{SS} = 0V$ ,  $T_a = -40$  to  $+85^\circ C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit	
			Min	Typ	Max		
HIGH-level output voltage	$V_{OH}$	Q: Measurement circuit 1, $I_{OH} = 6mA$	2.5	2.75	–	V	
LOW-level output voltage	$V_{OL}$	Q: Measurement circuit 1, $I_{OL} = 6mA$	–	0.2	0.4	V	
Output leakage current	$I_Z$	Q: Measurement circuit 6, INHN = LOW	$V_{OH} = V_{DD}$	–	–	10	$\mu A$
			$V_{OL} = V_{SS}$	–	–	10	$\mu A$
HIGH-level input voltage	$V_{IH}$	INHN	$0.7V_{DD}$	–	–	V	
LOW-level input voltage	$V_{IL}$	INHN	–	–	$0.3V_{DD}$	V	
Current consumption	$I_{DD}$	Measurement circuit 2, load circuit 1, INHN = open, $C_L = 15pF$ , $f = 37MHz$	CF5073D1	–	11	26	mA
			CF5073D2	–	9.5	24.5	mA
			CF5073D3	–	9	24	mA
			CF5073D4 to 6	–	8.5	23.5	mA
INHN pull-up resistance	$R_{UP}$	Measurement circuit 3	50	100	180	$k\Omega$	
Built-in resistance	$R_f$	Design value. A monitor pattern on a wafer is tested.	150	300	540	$k\Omega$	
	$R_D$		0.25	0.36	0.47	$k\Omega$	
	$R_{B1}$	Measurement circuit 4	100	200	360	$k\Omega$	
	$R_{B2}$	Design value. A monitor pattern on a wafer is tested.	50	100	180	$k\Omega$	
Built-in capacitance	$C_V$	Design value. A monitor pattern on a wafer is tested.	$V_C = 0.3V$	11.0	14.6	18.2	pF
			$V_C = 3.0V$	2.3	4.0	5.7	pF
	$C_G$	Design value. A monitor pattern on a wafer is tested.	25.5	30	34.5	pF	
	$C_D$		25.5	30	34.5	pF	
	$C_C$		34	40	46	pF	

**CF5073 series**

**CF5073E**×

$V_{DD} = 3.0$  to  $3.6V$ ,  $V_C = 1.65V$ ,  $V_{SS} = 0V$ ,  $T_a = -40$  to  $+85^\circ C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit	
			Min	Typ	Max		
HIGH-level output voltage	$V_{OH}$	Q: Measurement circuit 1, $I_{OH} = 6mA$	2.5	2.75	–	V	
LOW-level output voltage	$V_{OL}$	Q: Measurement circuit 1, $I_{OL} = 6mA$	–	0.2	0.4	V	
Output leakage current	$I_Z$	Q: Measurement circuit 6, INHN = LOW	$V_{OH} = V_{DD}$	–	–	10	$\mu A$
			$V_{OL} = V_{SS}$	–	–	10	$\mu A$
HIGH-level input voltage	$V_{IH}$	INHN	$0.7V_{DD}$	–	–	V	
LOW-level input voltage	$V_{IL}$	INHN	–	–	$0.3V_{DD}$	V	
Current consumption	$I_{DD}$	Measurement circuit 2, load circuit 1, INHN = open, $C_L = 15pF$ , $f = 44MHz$	CF5073E1	–	12	28	mA
			CF5073E2	–	10.5	26.5	mA
			CF5073E3	–	9.5	25.5	mA
			CF5073E4 to 6	–	9	25	mA
INHN pull-up resistance	$R_{UP}$	Measurement circuit 3	50	100	180	$k\Omega$	
Built-in resistance	$R_f$	Design value. A monitor pattern on a wafer is tested.	150	300	540	$k\Omega$	
	$R_D$		0.25	0.36	0.47	$k\Omega$	
	$R_{B1}$	Measurement circuit 4	100	200	360	$k\Omega$	
	$R_{B2}$	Design value. A monitor pattern on a wafer is tested.	50	100	180	$k\Omega$	
Built-in capacitance	$C_V$	Design value. A monitor pattern on a wafer is tested.	$V_C = 0.3V$	11.0	14.6	18.2	pF
			$V_C = 3.0V$	2.3	4.0	5.7	pF
	$C_G$	Design value. A monitor pattern on a wafer is tested.	21.2	25	28.8	pF	
	$C_D$		21.2	25	28.8	pF	
	$C_C$		42.5	50	57.5	pF	

**CF5073 series**

**CF5073F**×

$V_{DD} = 3.0$  to  $3.6V$ ,  $V_C = 1.65V$ ,  $V_{SS} = 0V$ ,  $T_a = -40$  to  $+85^\circ C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit	
			Min	Typ	Max		
HIGH-level output voltage	$V_{OH}$	Q: Measurement circuit 1, $I_{OH} = 6mA$	2.5	2.75	–	V	
LOW-level output voltage	$V_{OL}$	Q: Measurement circuit 1, $I_{OL} = 6mA$	–	0.2	0.4	V	
Output leakage current	$I_Z$	Q: Measurement circuit 6, INHN = LOW	$V_{OH} = V_{DD}$	–	–	10	$\mu A$
			$V_{OL} = V_{SS}$	–	–	10	$\mu A$
HIGH-level input voltage	$V_{IH}$	INHN	$0.7V_{DD}$	–	–	V	
LOW-level input voltage	$V_{IL}$	INHN	–	–	$0.3V_{DD}$	V	
Current consumption	$I_{DD}$	Measurement circuit 2, load circuit 1, INHN = open, $C_L = 15pF$ , $f = 51MHz$	CF5073F1	–	13	30	mA
			CF5073F2	–	11	28	mA
			CF5073F3	–	10	27	mA
			CF5073F4 to 6	–	9.5	26.5	mA
INHN pull-up resistance	$R_{UP}$	Measurement circuit 3	50	100	180	$k\Omega$	
Built-in resistance	$R_f$	Design value. A monitor pattern on a wafer is tested.	150	300	540	$k\Omega$	
	$R_D$		0.25	0.36	0.47	$k\Omega$	
	$R_{B1}$	Measurement circuit 4	100	200	360	$k\Omega$	
	$R_{B2}$	Design value. A monitor pattern on a wafer is tested.	50	100	180	$k\Omega$	
Built-in capacitance	$C_V$	Design value. A monitor pattern on a wafer is tested.	$V_C = 0.3V$	9.5	12.5	15.5	pF
			$V_C = 3.0V$	2.0	3.5	5.0	pF
	$C_G$	Design value. A monitor pattern on a wafer is tested.	17	20	23	pF	
	$C_D$		17	20	23	pF	
	$C_C$		42.5	50	57.5	pF	

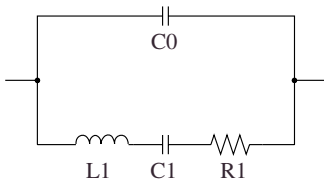
## SWITCHING CHARACTERISTICS

$V_{DD} = 3.0$  to  $3.6V$ ,  $V_C = 1.65V$ ,  $V_{SS} = 0V$ ,  $T_a = -40$  to  $+85^\circ C$ , unless otherwise noted

Parameter	Symbol	Conditions	Rating <sup>1</sup>			Unit
			Min	Typ	Max	
Output rise time	$t_{r1}$	Measurement circuit 2, load circuit 1, $0.1V_{DD} \rightarrow 0.9V_{DD}$ , $C_L = 15pF$	–	2.5	6	ns
Output fall time	$t_{f1}$	Measurement circuit 2, load circuit 1, $0.9V_{DD} \rightarrow 0.1V_{DD}$ , $C_L = 15pF$	–	2.5	6	ns
Output duty cycle	Duty	Measurement circuit 2, load circuit 1, $V_{DD} = 3.3V$ , $T_a = 25^\circ C$ , $C_L = 15pF$	40	50	60	%
Output disable delay time	$t_{PLZ}$	Measurement circuit 5, load circuit 1, $V_{DD} = 3.3V$ , $T_a = 25^\circ C$ , $C_L \leq 15pF$	–	–	100	ns
Output enable delay time	$t_{PZL}$		–	–	100	ns

1. The switching characteristics apply for normal output waveforms. Note that, depending on the matching of the CF5073 series version and crystal, normal waveform output may not be continuous.

## Current consumption and Output waveform with NPC's standard crystal



f [MHz]	R1 [ $\Omega$ ]	L1 [mH]	C1 [fF]	C0 [pF]
30	7.06	2.25	12.5	3.11

## FUNCTIONAL DESCRIPTION

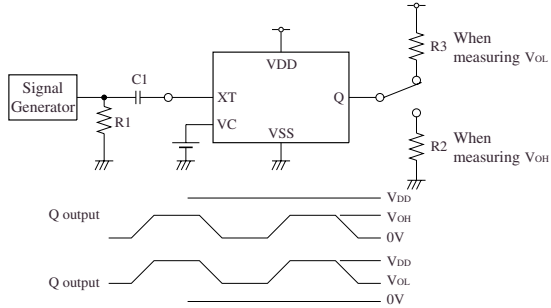
### Standby Function

When INHN goes LOW, the Q output pin becomes high impedance.

INHN	Q	Oscillator
HIGH (or open)	Any $f_O$ , $f_O/2$ , $f_O/4$ , $f_O/8$ , $f_O/16$ , or $f_O/32$	Operating
LOW	High impedance	Operating

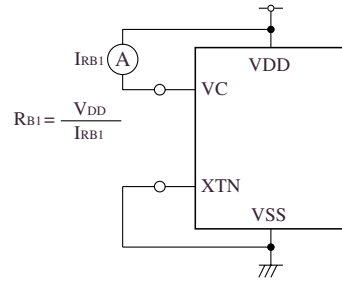
**MEASUREMENT CIRCUITS**

**Measurement Circuit 1**

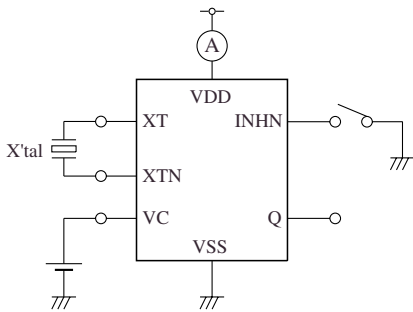


XT input signal: 2.5Vp-p, 10MHz, sine wave  
 $C1 = 0.001\mu\text{F}$ ,  $R1 = 50\Omega$ ,  $R2 = 417\Omega$ ,  $R3 = 434\Omega$ ,  $V_C = 1.65\text{V}$

**Measurement Circuit 4**

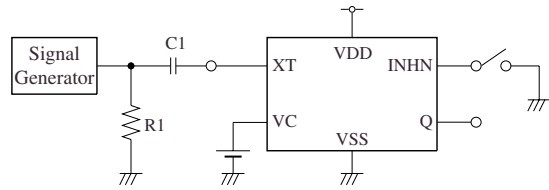


**Measurement Circuit 2**



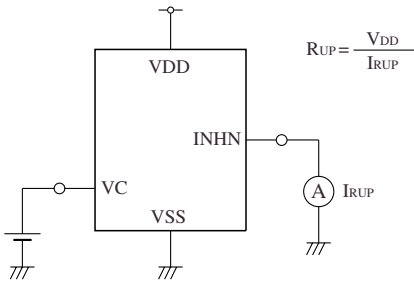
$V_C = 1.65\text{V}$ , INHN = open, crystal oscillation

**Measurement Circuit 5**



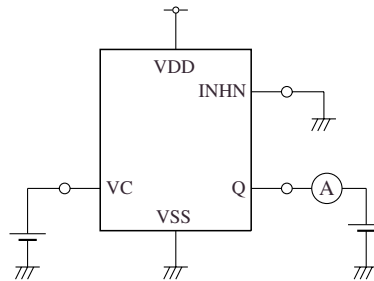
XT input signal: 2.5Vp-p, 10MHz, sine wave  
 $C1 = 0.001\mu\text{F}$ ,  $R1 = 50\Omega$ ,  $V_C = 1.65\text{V}$

**Measurement Circuit 3**



$V_C = 1.65\text{V}$

**Measurement Circuit 6**



$V_C = 1.65\text{V}$



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The logo for SEIKO NPC CORPORATION, consisting of the letters 'NPC' in a bold, black, sans-serif font.

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