

**OVERVIEW**

The SM5300AV is a video buffer with built-in video signal bandwidth lowpass filter. The filter employs a 5-order Butterworth lowpass filter configuration. The filter characteristics have been optimized for minimal overshoot and flat group delay, it has a variable cutoff frequency and guaranteed driver-stage channel gain difference and phase difference values. The output gain for each channel can be set independently, making it possible to adjust the gain difference between channels.

**FEATURES**

- Supply voltage: 5V ± 10%
- VESA-standard ATSC digital TV RGB/YUV video filters
- 2-system input/1-system output switching analog multiplexer function
- DC voltage level restore sync clamp function
- Output buffer gain switching function: 0 (× 1), 3 to 10dB (input-to-output AC signal gain)
- Channel-to-channel gain difference: 0.4%
- Channel-to-channel phase difference: 0.4°
- Output signal harmonic distortion (all channels): 0.8%
- Cutoff frequency: 5 to 40MHz variable
- Package: 28-pin VSOP

**APPLICATIONS**

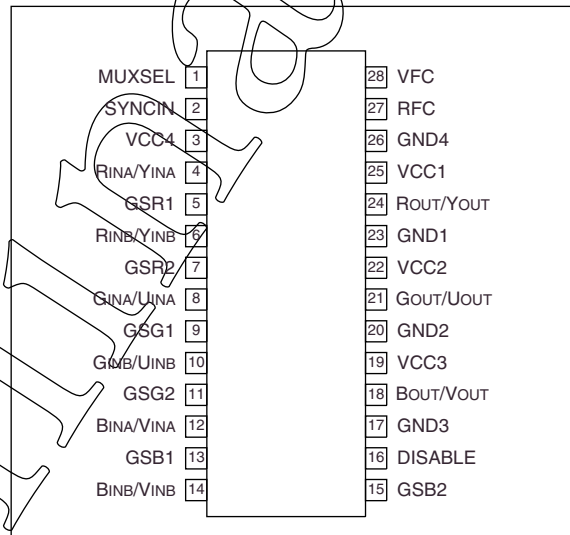
- Set-top boxes
- Digital television
- DVD players

**ORDERING INFORMATION**

Device	Package
SM5300AV	28-pin VSOP

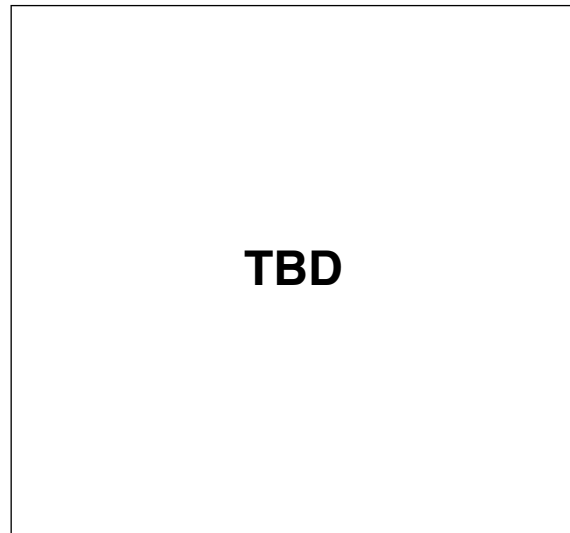
**PINOUT**

(Top View)

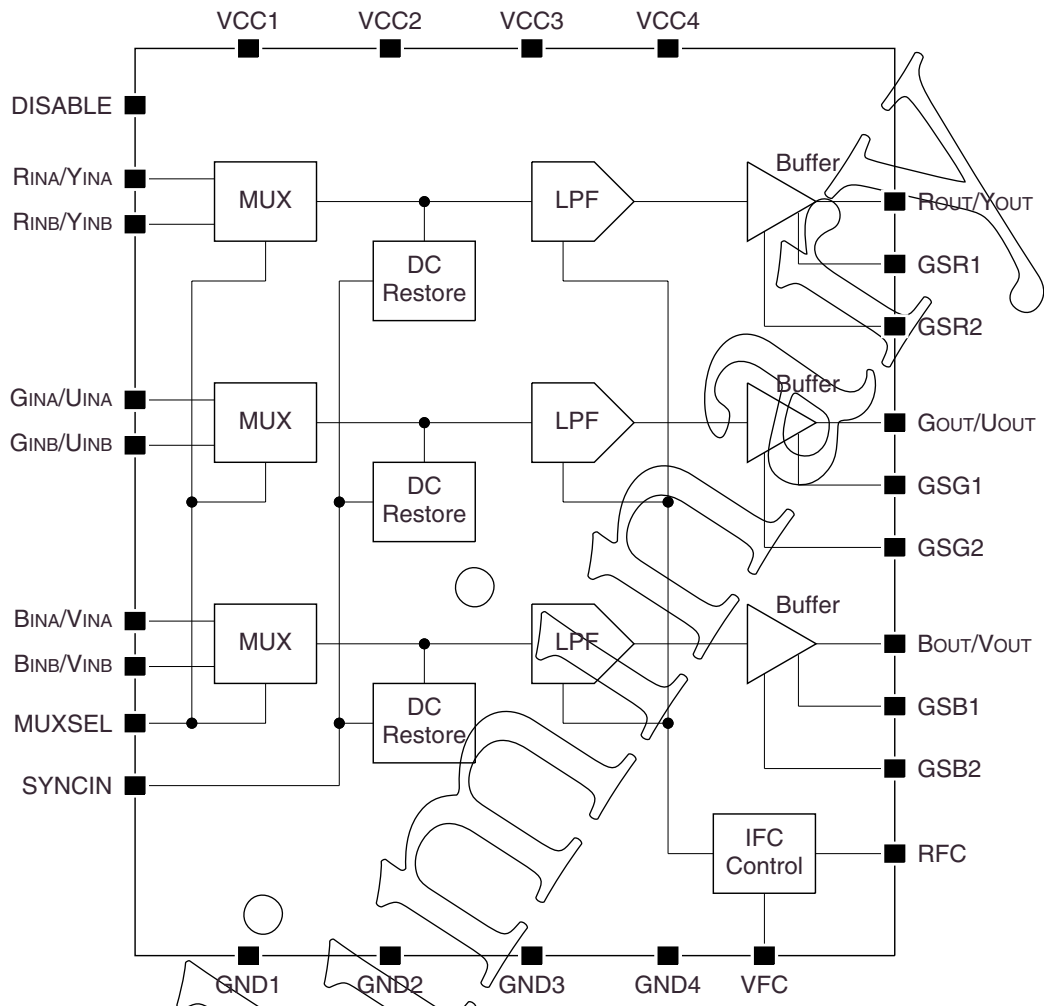


**PACKAGE DIMENSIONS**

(Unit: mm)



**BLOCK DIAGRAM**



Pre-Release

## PIN DESCRIPTION

Number	Name	I/O	Description
1	MUXSEL	I	Input select signal. Built-in pull-down resistor. L: $\times_{INA}$ pin select, H: $\times_{INB}$ pin select
2	SYNCIN	I	Filter channel external H-Sync signal input. Active "H". Built-in pull-down resistor.
3	VCC4	—	Analog 5V supply
4	$R_{INA}/Y_{INA}$	I	Analog $R_{INA}$ or $Y_{INA}$ signal input. Sync signal is input on SYNCIN pin.
5	GSR1	I	$R_{OUT}/Y_{OUT}$ output buffer gain set input
6	$R_{INB}/Y_{INB}$	I	Analog $R_{INB}$ or $Y_{INB}$ signal input. Sync signal is input on SYNCIN pin.
7	GSR2	I	$R_{OUT}/Y_{OUT}$ output buffer gain set input
8	$G_{INA}/U_{INA}$	I	Analog $G_{INA}$ or $U_{INA}$ signal input. Sync signal is input on SYNCIN pin.
9	GSG1	I	$G_{OUT}/U_{OUT}$ output buffer gain set input
10	$G_{INB}/U_{INB}$	I	Analog $G_{INB}$ or $U_{INB}$ signal input. Sync signal is input on SYNCIN pin.
11	GSG2	I	$G_{OUT}/U_{OUT}$ output buffer gain set input
12	$B_{INA}/V_{INA}$	I	Analog $B_{INA}$ or $V_{INA}$ signal input. Sync signal is input on SYNCIN pin.
13	GSB1	I	$B_{OUT}/V_{OUT}$ output buffer gain set input
14	$B_{INB}/V_{INB}$	I	Analog $B_{INB}$ or $V_{INB}$ signal input. Sync signal is input on SYNCIN pin.
15	GSB2	I	$B_{OUT}/V_{OUT}$ output buffer gain set input
16	DISABLE	I	Power save function. Built-in pull-down resistor. L: Enable, H: Disable
17	GND3	—	Analog ground
18	$B_{OUT}/V_{OUT}$	O	B/V signal output
19	VCC3	—	Analog 5V supply
20	GND2	—	Analog ground
21	$G_{OUT}/U_{OUT}$	O	G/U signal output
22	VCC2	—	Analog 5V supply
23	GND1	—	Analog ground
24	$R_{OUT}/Y_{OUT}$	O	R/Y signal output
25	VCC1	—	Analog 5V supply
26	GND4	—	Analog ground
27	RFC	—	LPF (lowpass filter) cutoff frequency setting resistor connection
28	VFC	I	LPF (lowpass filter) cutoff frequency setting voltage input

## SPECIFICATIONS

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	- 0.3 to 7.0	V
Input voltage range	$V_{IN}$	- 0.3 to $V_{CC} + 0.3$	V
Storage temperature range	$T_{stg}$	- 55 to + 125	°C
Power dissipation	$P_D$	TBD	mW

### Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply voltage ranges	$V_{CC}$	4.5 to 5.5	V
Operating temperature range	$T_{opr}$	0 to 70	°C

### Electrical Characteristics

$V_{CC} = 4.5$  to  $5.5V$ ,  $T_a = 0$  to  $70^\circ C$  unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Supply current 1	$I_{CC1}$	$V_{CC} = 5.5V$ , RFC: $1.2k\Omega$ to GND, VFC = $0.2V$ ( $f_c = 5MHz$ ), DISABLE = "L"		72		mA	I
Supply current 2	$I_{CC2}$	$V_{CC} = 5.5V$ , RFC: $1.2k\Omega$ to GND, VFC = $1.6V$ ( $f_c = 40MHz$ ), DISABLE = "L"		100		mA	I
Supply current 3	$I_{CC3}$	$V_{CC} = 5.5V$ , RFC: $1.2k\Omega$ to GND, DISABLE = "H", Other I/O pins are open.		2.3		mA	I
Gain adjust range	$A_V$	Measured at DC (see table 1)	0		10	dB	I
Output gain error	$\Delta A_V$	Error entered around table 1 values			$\pm 1$	dB	I
Output voltage	$V_{out2}$	$R_L = 75\Omega$ to GND	2.4			Vp-p	I
DISABLE-mode input impedance	$R_{IN1}$	$R_{INA}/Y_{INA}$ , $R_{INB}/Y_{INB}$ , $G_{INA}/U_{INA}$ , $G_{INB}/U_{INB}$ , $B_{INA}/V_{INA}$ , $B_{INB}/V_{INB}$		50		$k\Omega$	I
Clamp response time	$T_{clamp}$	Time for output signal to change by 90%, Input signal = $10mV$ , $C_{IN} = 0.1\mu F$		1		ms	II
Maximum input amplitude	$V_I$	AC coupling		1.4		Vp-p	II
Maximum overshoot	$V_{OS}$	2Vp-p output pulse		4.3		%	II
Maximum load capacitance	$C_L$	$B_{OUT}/V_{OUT}$ , $G_{OUT}/U_{OUT}$ , $R_{OUT}/Y_{OUT}$			35	pF	II
Output drive load	$R_L$	one load unit = $150\Omega$		2		load	I
Channel-to-channel gain difference	dG	Between R/G/B, $f_c/2$ [Hz]		0.4		%	I
Channel-to-channel phase difference	d $\phi$	Between R/G/B, $f_c/2$ [Hz]		0.4		degree	II
Output harmonic distortion	$T_{HD}$	$V_{out} = 2Vp-p$ , $f = 1MHz$		0.8		%	II
Power supply rejection ratio	PSRR	$V_{CC} = 0.5Vp-p$ , $f = 100kHz$		35		dB	II

## SM5300AV

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Output short-circuit current	$I_{SC}$				100	mA	II
Logic HIGH-level input voltage 1	$V_{IH1}$	DISABLE, MUXSEL, SYNCIN	2.5			V	I
Logic LOW-level input voltage 1	$V_{IL1}$	DISABLE, MUXSEL, SYNCIN			1.0	V	I
Logic HIGH-level input voltage 2	$V_{IH2}$	GSB1, GSB2, GSG1, GSG2, GSR1, GSR2	$V_{CC} - 0.5$			V	I
Logic LOW-level input voltage 2	$V_{IL2}$	GSB1, GSB2, GSG1, GSG2, GSR1, GSR2			0.5	V	I
Logic open-circuit voltage	$V_{OPEN}$	GSB1, GSB2, GSG1, GSG2, GSR1, GSR2	$V_{CC}/2 - 0.5$		$V_{CC}/2 + 0.5$	V	I
Logic pull-down resistance	$R_{IN2}$	DISABLE, MUXSEL, SYNCIN		50		k $\Omega$	I

### Filter Characteristics

$V_{CC} = 4.5$  to  $5.5V$ ,  $T_a = 0$  to  $70^\circ C$  unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Cutoff frequency adjustment range	$F_C$	$T_a = 25^\circ C$ (see figure 2)	5.0		40	MHz	I
Cutoff frequency error	$\Delta F_C$	$T_a = 25^\circ C$			$\pm 20$	%	I
4fc attenuation	$f_{SB}$	$f_{IN} \geq 4f_c$		50		dB	II
Output noise characteristic	$V_{NOISE}$	10kHz to 40MHz, Output gain = 6dB		1.0		mV <sub>RMS</sub>	II
Crosstalk	$X_{TALK}$	Between 2 channels with input 0.5V <sub>p-p</sub> 1MHz		-55		dB	II
Multiplexer crosstalk	$X_{TALK}$	Between MUX A-B		-54		dB	II
Channel-to-channel group delay	$T_{PD}$	Each input = 100kHz		16		ns	II
Group delay variation	$\Delta T_{PD1}$	Fc = 6.7MHz (100kHz)	to 3.58MHz	4		ns	II
			to 4.43MHz	8		ns	II
			to 10MHz	9		ns	II
	$\Delta T_{PD2}$	Fc = 27MHz (100kHz)	to 3.58MHz	1		ns	II
			to 4.43MHz	1		ns	II
			to 10MHz	2		ns	II
$\Delta T_{PD3}$	Fc = 36MHz (100kHz)	to 10MHz	0.5		ns	II	
		to 30MHz	4		ns	II	
VFC input voltage range	VFC		0.1		2	V	I

Test level

I: 100% of products tested at  $T_a = +25^\circ C$ .

II: Guaranteed as result of design and characteristics evaluation.

Table 1. Output buffer gain control

GS×1	GS×2	Gain [dB]
GND	Open	0
GND	GND	3
Open	GND	4
VCC	GND	5
Open	Open	6
GND	VCC	7
Open	VCC	8
VCC	VCC	9
VCC	Open	10

R<sub>OUT</sub>/Y<sub>OUT</sub> gain setting using both GSR1 and GSR2 in combination (similarly for GSB1 and GSB2, GSG1 and GSG2)

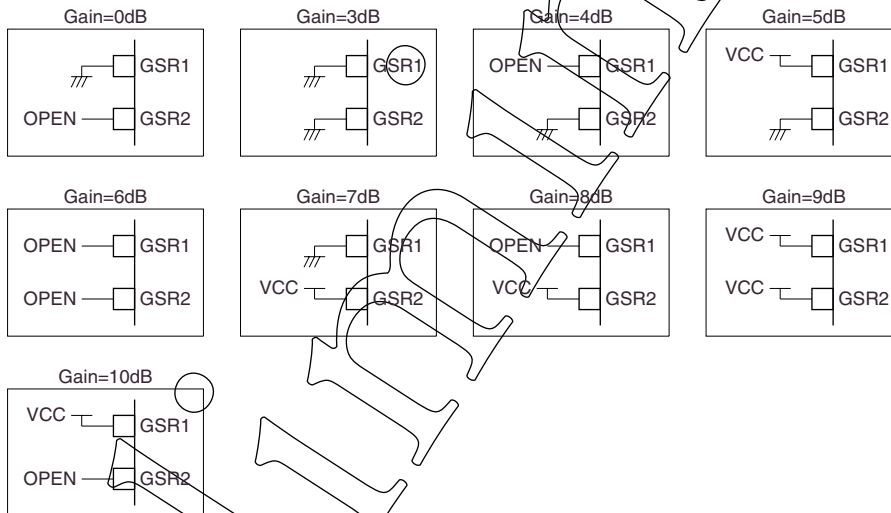


Figure 1. Setting the gain using GS×1 and GS×2

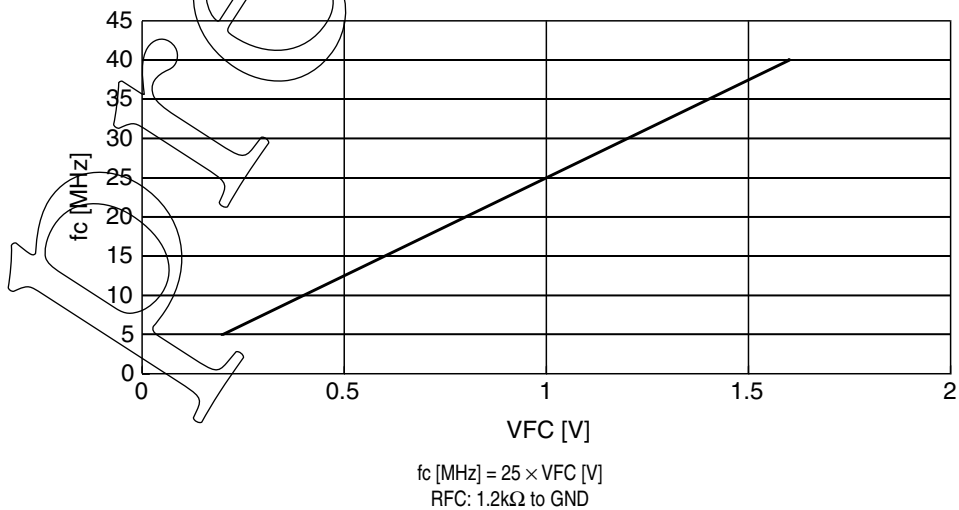
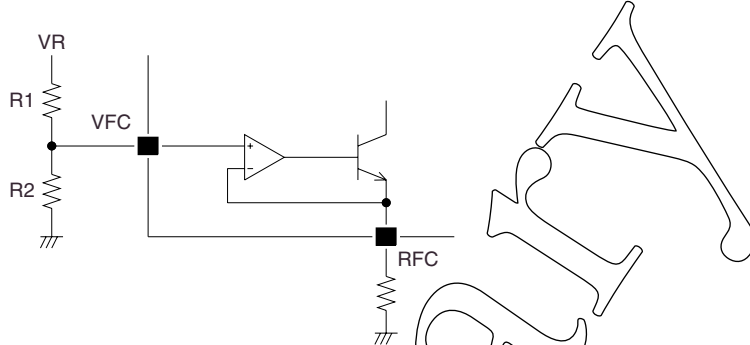


Figure 2. VFC vs. cutoff frequency

## Adjusting the Cutoff Frequency

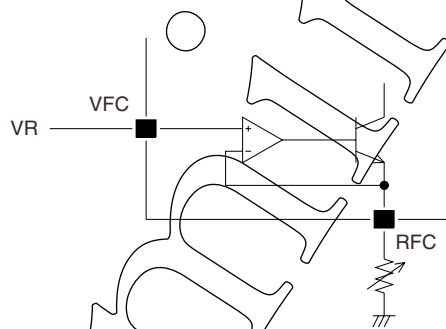
### Constant-voltage control 1

Cutoff frequency control using a reference voltage  $V_R$  generated by voltage divider formed by  $R_1$  and  $R_2$ .



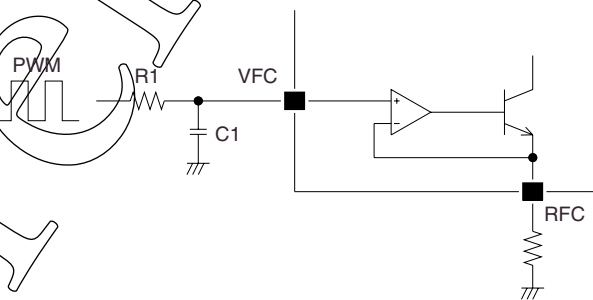
### Constant-voltage control 2

Cutoff frequency control by adjusting the resistance connected to  $R_{FC}$ .



### PWM control

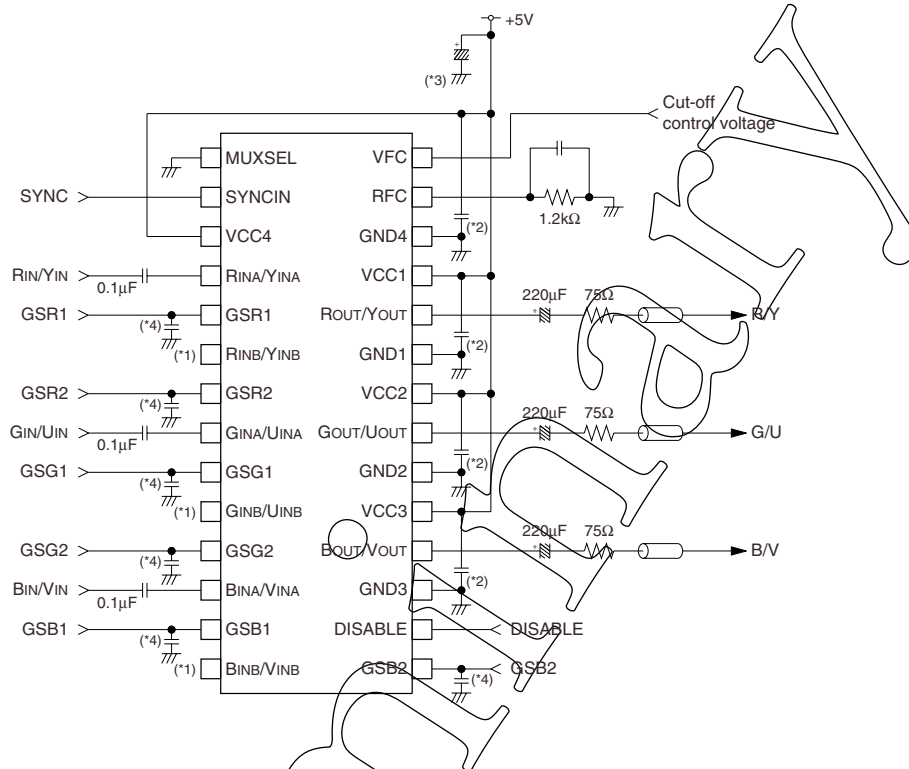
Cutoff frequency control by smoothing the PWM signal, using  $R_1$  and  $C_1$ , input to  $V_{FC}$ .



Note: The accuracy of the resistance connected to  $R_{FC}$  affects the cutoff frequency characteristic, thus a high-precision resistor should be used.

## TYPICAL APPLICATION CIRCUITS

### ATSC Digital TV Application



- (\*1) Pins without an input signal, set by NUXSEL, should be left open or tied to GND.
- (\*2) Connect  $4 \times 0.1\mu\text{F}$  capacitor between the supply pins close to the IC.
- (\*3) Connect a  $47\mu\text{F}$  capacitor between the supply pins close to the IC.
- (\*4) GS $\times$ 1 and GS $\times$ 2 are 3-level pins. Connect a capacitor if an error occurs due to external noise. Also, if open-circuit, the internal impedance and external capacitance (C) form an RC network. When power is applied, the open-circuit potential rises with time constant  $\tau = C \times 10\text{k}$  (sec).
- (\*5) Printed circuit board supply wiring
- If the supply is used for other digital circuits, there is a possibility that noise will be introduced. Accordingly, these circuits should be connected to the application's analog supply.
  - Ground-plane wiring should be performed, as much as possible, to provide low GND line impedance.
  - If ground-plane wiring up to the GND pins is difficult, the ground plane should be as close to the IC as possible with a separate wire to each GND pin.

### Input Capacitor and Cutoff Frequency

The capacitor connected to pins  $R_{INA}/Y_{INA}$ ,  $R_{INB}/Y_{INB}$ ,  $G_{INA}/U_{INB}$ ,  $G_{INB}/U_{INB}$ ,  $B_{INA}/V_{INA}$ , and  $B_{INB}/V_{INB}$  forms a highpass filter (HPF) with the internal impedance.

The HPF cutoff frequency is given by the following equation.

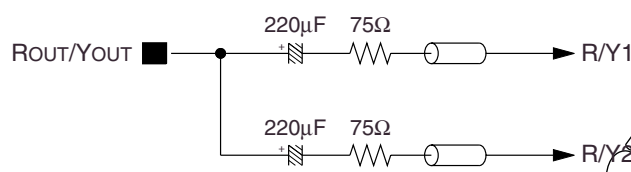
$$f_c = \frac{1}{2\pi CR}$$

(C = input capacitance, R = input impedance)

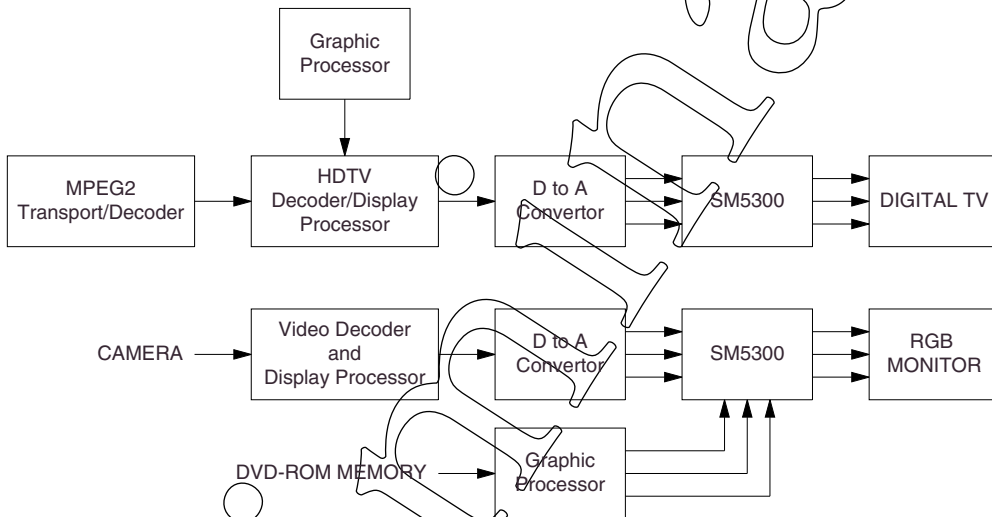
Note: Input impedance = TBD

**2-load Output Connection**

R<sub>OUT</sub>/Y<sub>OUT</sub> output 2-load connection (similarly for G<sub>OUT</sub>/U<sub>OUT</sub>, B<sub>OUT</sub>/V<sub>OUT</sub> outputs)



**Digital TV Receiver and HDTV Decoder Box**



Preliminary

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