

**OVERVIEW**

The SM5305A is a 75Ω terminating resistance drive video buffer with built-in analog filter. The output buffer can be selected 6dB and 12dB. The coupling capacitances can be reduced since the sag compensation circuit built-in. The device operates from 2.7 to 3.6V supply voltage. The cutoff frequency of lowpass filter is 6.75MHz.

**FEATURES**

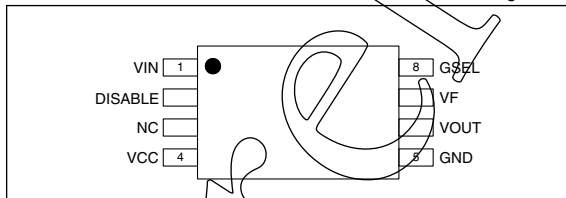
- Supply voltage: 2.7 to 3.6V
- Current consumption
  - 9.5mA when enable ( $V_{CC} = 3.0V$ )
  - < 1μA when disable
- Lowpass filter characteristics
  - 6.75MHz cutoff frequency (−3dB)
  - $\leq \pm 15\%$  cutoff frequency error
- Output buffer gain switching function: 6, 12dB
- Output gain error:  $\pm 0.5dB$  (Gain = 6dB)
- $\pm 0.7dB$  (Gain = 12dB)
- Sag compensation circuit built-in
- Operating temperature range: −20 to 70°C
- Package: 8-pin VSOP (Pb free)
- 8-pin PLP (Pb free)

**APPLICATIONS**

- Digital still camera
- Digital video camera
- Other portable equipment

**PINOUT**

(Top view)



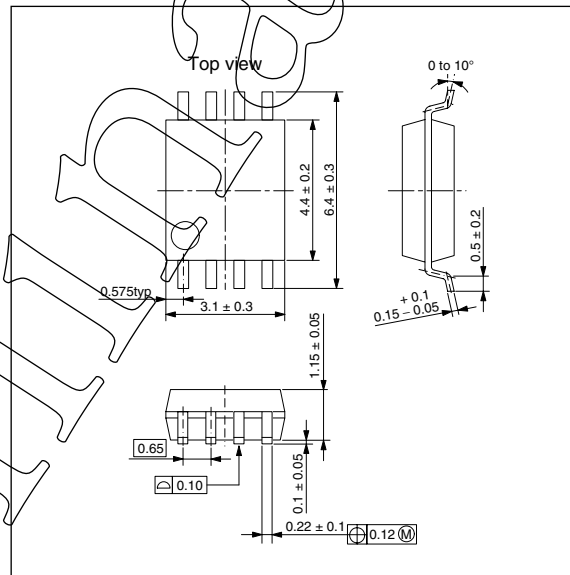
**ORDERING INFORMATION**

Device	Package
SM5305AV	8-pin VSOP
SM5305AD	8-pin PLP

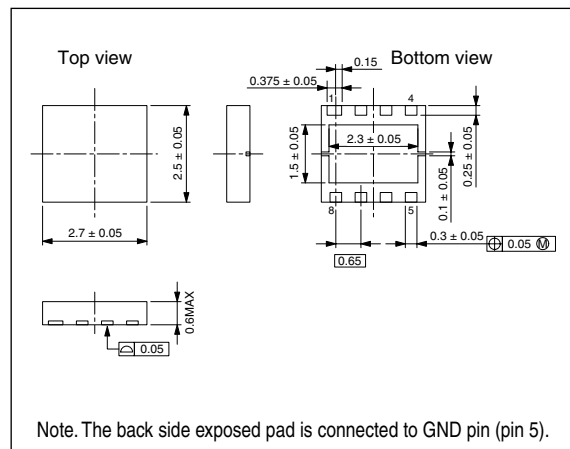
**PACKAGE DIMENSIONS**

(Unit: mm)

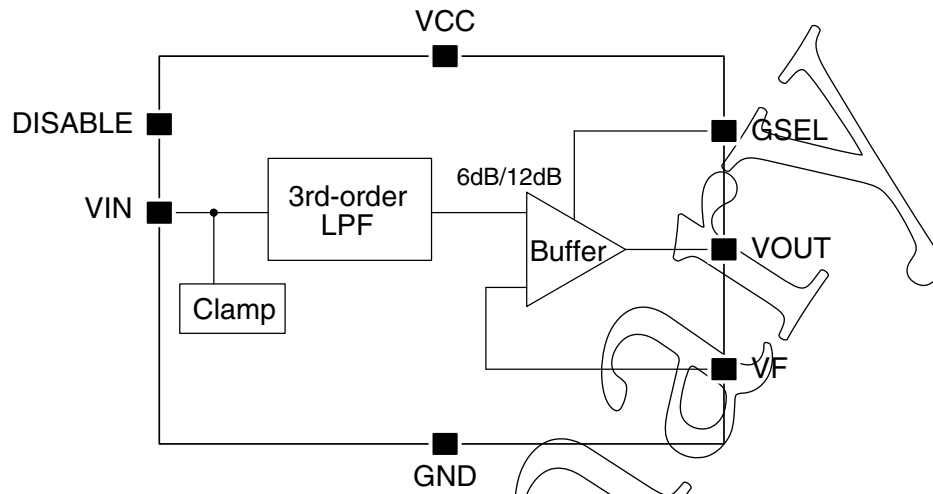
■ 8-pin VSOP



■ 8-pin PLP



## BLOCK DIAGRAM



## PIN DESCRIPTION

Number	Name	I/O <sup>1</sup>	A/D <sup>2</sup>	Description
1	VIN	I	A	Video signal input pin
2	DISABLE	I	D	Disable set pin (LOW: enable, HIGH: disable)
3	NC	-	-	No connection
4	VCC	-	-	Supply pin
5	GND	-	-	Ground pin
6	VOUT	O	A	Video signal output pin
7	VF	I	A	Output signal feedback pin for sag compensation circuit
8	GSEL	I	D	Gain switching set pin (LOW: 6dB, HIGH: 12dB)

1. I: input, O: output  
2. A: analog, D: digital

PIN EQUIVALENT CIRCUITS

Number	Name	I/O	Equivalent circuit
1	VIN	I	
8	GSEL	I	
2	DISABLE	I	
6 7	VOUT VF	O I	

## SPECIFICATIONS

### Absolute Maximum Ratings

GND = 0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	$V_{CC}$		-0.3 to 7.0	V
Input voltage range	$V_{IN}$	GSEL, DISABLE pins	GND - 0.3 to $V_{CC} + 0.3$	V
Storage temperature range	$T_{stg}$		-55 to 125	°C
Power dissipation	$P_D$	VSOP package	300	mW
		PLP package	320	mW

### Recommended Operating Conditions

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	$V_{CC}$		2.7 to 3.6	V
Operating temperature range	$T_a$		-20 to 70	°C

### DC Characteristics (GSEL, DISABLE)

$V_{CC} = 2.7$  to  $3.6$ V,  $T_a = -20$  to  $70$ °C, unless otherwise noted.

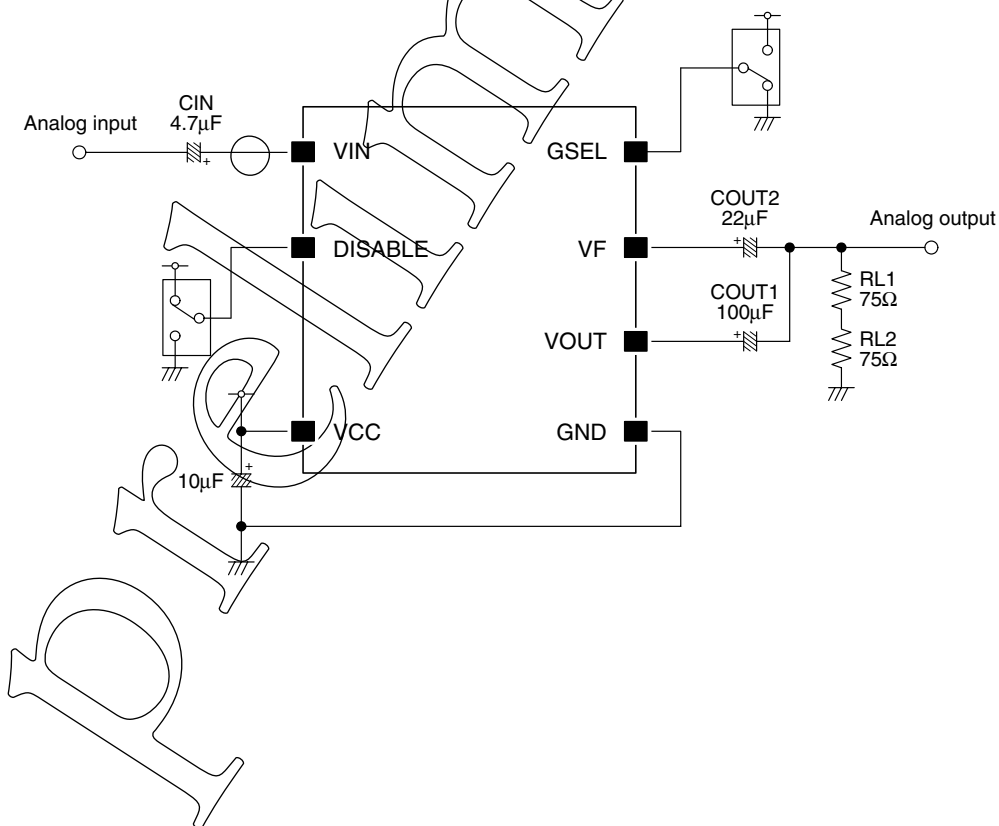
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level input voltage	$V_{IH}$		$0.7V_{CC}$	-	-	V
LOW-level input voltage	$V_{IL}$		-	-	0.5	V
Input leakage current	$I_{LL}$	$V_{IN} = 0V$	-	-	1	μA
	$I_{LH}$	$V_{IN} = V_{CC}$	-	-	1	μA

### Analog Characteristics

$V_{CC} = 3.0V$ ,  $T_a = 25^{\circ}C$ ,  $R_L = 150\Omega$ ,  $f_{in} = 100kHz$ , unless otherwise noted.  
Refer to "Measurement Circuit Diagram".

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption 1	$I_{CC1}$	$V_{CC} = 2.7$ to $3.6V$	-	9.5	16	mA
Current consumption 2	$I_{CC2}$	$V_{CC} = 2.7$ to $3.6V$ when DISABLE	-		1	$\mu A$
Output gain 1	$A_{V1}$	Gain = 6dB	5.5	6.0	6.5	dB
Output gain 2	$A_{V2}$	Gain = 12dB	11.3	12.0	12.7	dB
Input voltage range 1	$V_{AIN1}$	Gain = 6dB	-	-	1.2	Vp-p
Input voltage range 2	$V_{AIN2}$	Gain = 12dB	-	-	0.6	Vp-p
Maximum output voltage	$V_{out}$	THD < 1.5%	2.0	2.4	-	Vp-p
Input clamp voltage	$V_{CLMP}$	VIN pin, AC-coupled input	0.8	1.0	1.2	V
Output harmonic distortion	$T_{HD}$	$V_{OUT} = 2V_{p-p}$	-	1.0	-	%
Frequency characteristics	4fc	$f_{in} = 27MHz/100kHz$	-	-37	-33	dB
Cutoff frequency	$F_C$	-3dB ( $f_{in} = 100kHz$ )	5.7	6.75	7.8	MHz
Group delay difference	$\Delta GD$	100kHz and 5MHz group delay difference	-	15	-	ns

### Measurement Circuit Diagram





**TYPICAL CHARACTERISTICS**

$V_{CC} = 3.0V$ ,  $T_a = 25^\circ C$ ,  $R_L = 150\Omega$ ,  $f_{in} = 100kHz$ , unless otherwise noted.

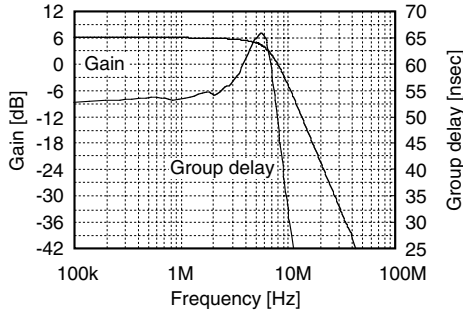


Figure 1. Filter characteristics (Gain = 6dB)

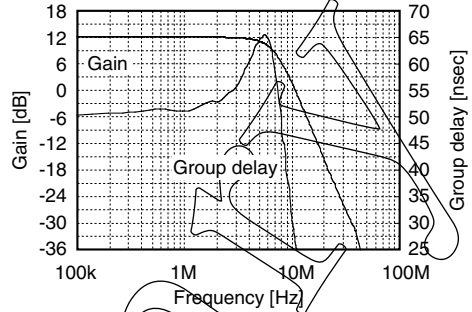


Figure 2. Filter characteristics (Gain = 12dB)

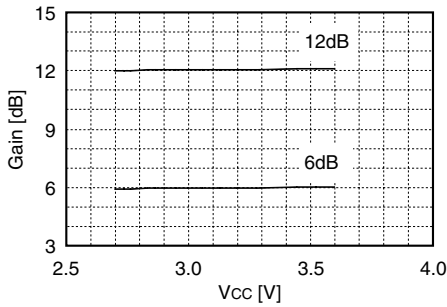


Figure 3. Gain vs.  $V_{CC}$

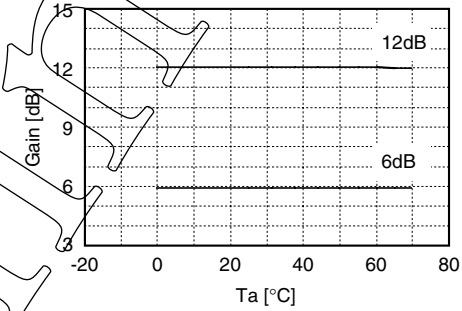


Figure 4. Gain vs.  $T_a$

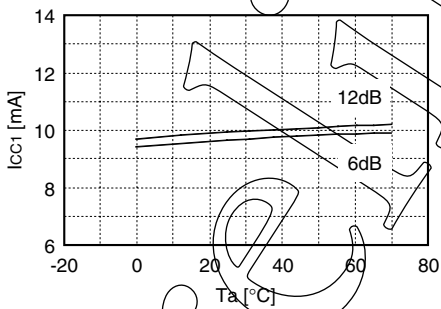


Figure 5.  $I_{CC1}$  vs.  $T_a$

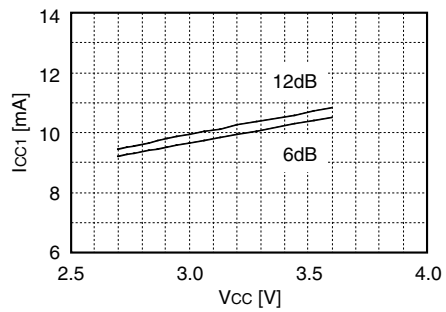


Figure 6.  $I_{CC1}$  vs.  $V_{CC}$

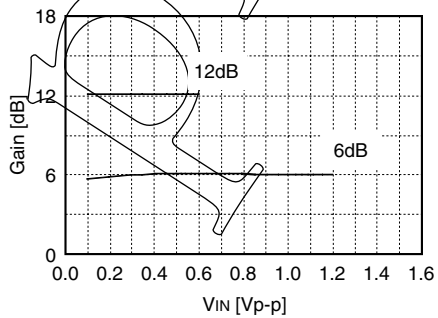


Figure 7. Gain vs.  $V_{IN}$

Preliminary

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NP0204DE 2004.09