

### OVERVIEW

The SM5865CM is a 24-bit input D/A converter LSI for high-quality digital audio equipment. It comprises newly developed DEM (dynamic element matching) circuits, 3rd-order  $\Sigma\Delta$  noise shaper and 31-level quantizer to realize super low total harmonic distortion and wide dynamic range. Also, the device is widely reduced residual quantization noise up to high-frequency bandwidth in the audio band so the order of the required final-stage analog lowpass filter can be reduced, making it ideal for application with high-frequency sampling format. The output stage employs differential current outputs for high-accuracy analog signals, with appropriate lowpass filtering of the output signal.

This device can be used in combination with an 8-times oversampling digital filter of SM5847AF and others like that for the compatibility with 192kHz sampling format.

### FEATURES

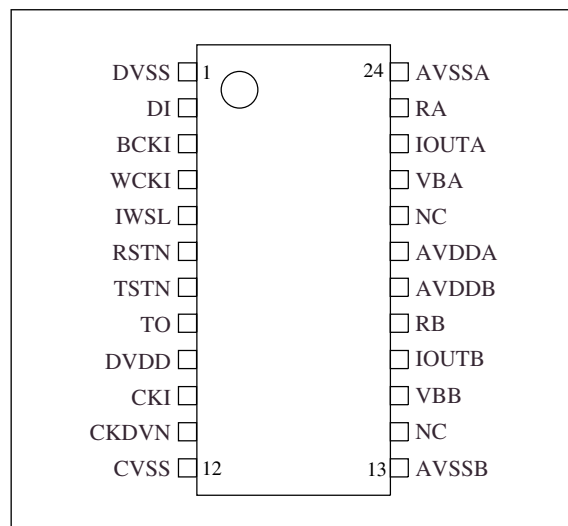
- Mono-channel D/A converter LSI
- High performance
  - 0.00030% (−110.5dB) typ. THD + N
  - 117dB typ. Dynamic range
  - 120dB typ. S/N
- Input interface
  - 20 or 24-bit word length
  - MSB first, right-justified format
  - 8 or 4 times oversampling at  $f_s = 16/32/44.1/48/88.2/96/176.4/192\text{kHz}$
- System clock frequency
  - 192/256/384/512/768/1024fs
- Single 5V operating supply voltage
- Molybdenum-gate CMOS process
- 24-pin SSOP package

### ORDERING INFORMATION

Device	Package
SM5865CM	24-pin SSOP

### PINOUT

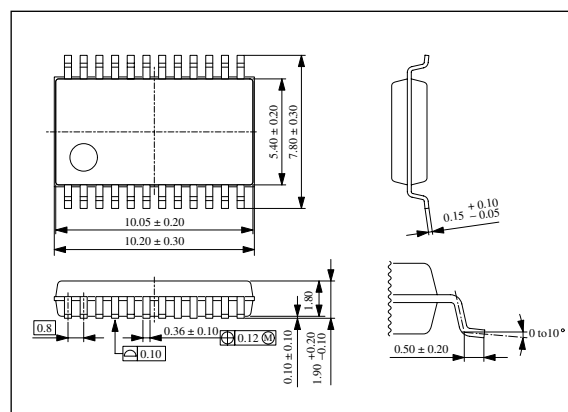
(Top view)



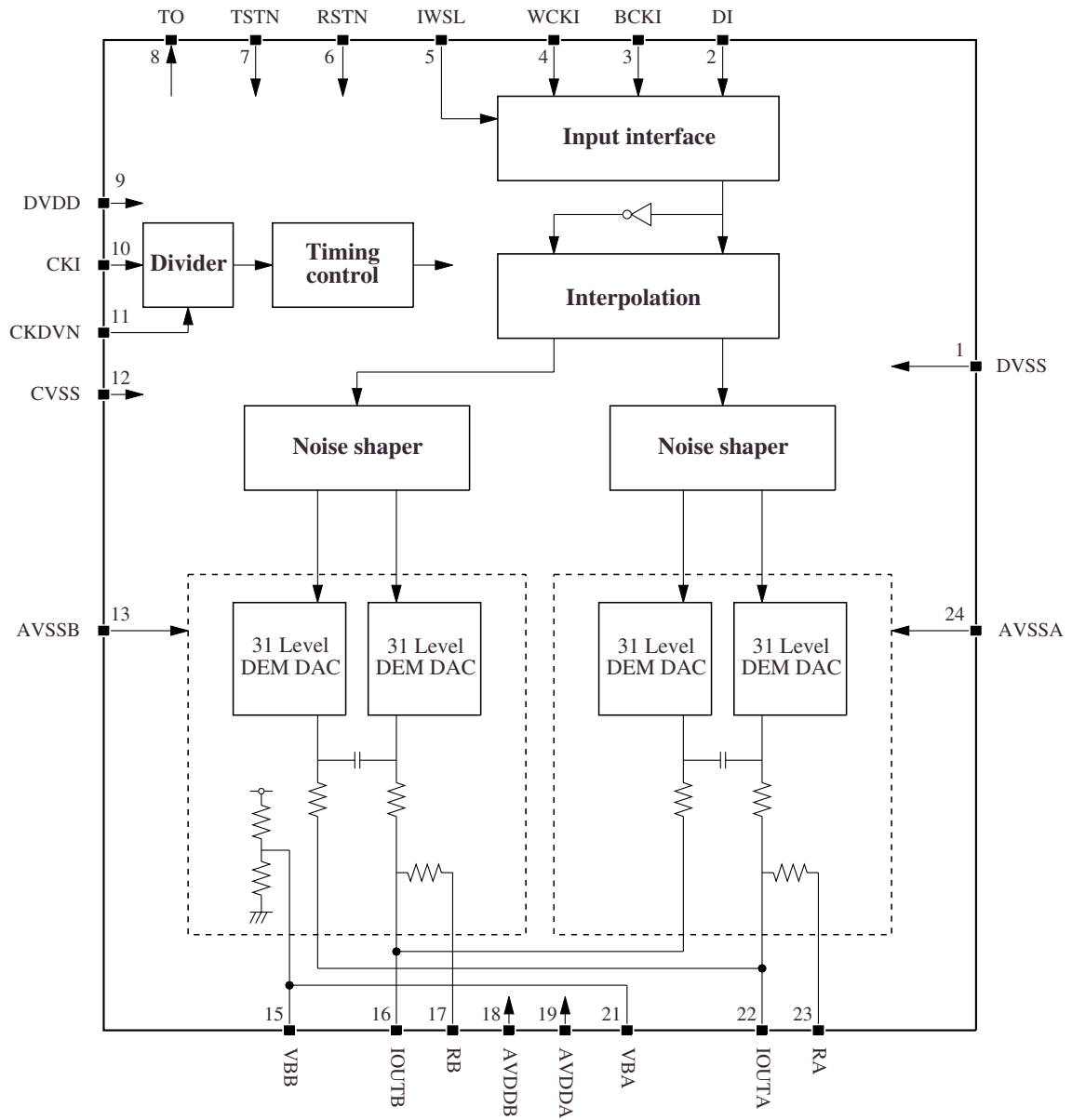
### PACKAGE DIMENSIONS

(Unit: mm)

Weight: 0.23g



**BLOCK DIAGRAM**



## PIN DESCRIPTION

Number	Name	I/O <sup>1</sup>	Description
1	DVSS	–	Digital ground
2	DI	I	Data input
3	BCKI	I	Bit clock input
4	WCKI	I	Word clock input
5	IWSL	I <sub>p</sub>	Input data word length select. 24-bit when HIGH, and 20-bit when LOW.
6	RSTN	I <sub>p</sub>	System reset. Reset when LOW.
7	TSTN	I <sub>p</sub>	Test pin. Tie HIGH or leave open for normal operation.
8	TO	O	Test output
9	DVDD	–	Digital supply
10	CKI	I	System clock input
11	CKDVN	I <sub>p</sub>	System clock frequency divider ratio select. 1 when HIGH (no division), and 2 when LOW (half of the input frequency).
12	CVSS	–	System clock ground
13	AVSSB	–	Analog ground B
14	NC	–	Leave open for no connection or connect with ground
15	VBB	O	1/2 supply output B
16	IOUTB	O	Inverse-phase analog output B
17	RB	I	Built-in resistor connection B
18	AVDDB	–	Analog supply B
19	AVDDA	–	Analog supply A
20	NC	–	Leave open for no connection or connect with ground
21	VBA	O	1/2 supply output A
22	IOUTA	O	In-phase analog output A
23	RA	I	Built-in resistor connection A
24	AVSSA	–	Analog ground A

1. I<sub>p</sub> : Pull-up input

## SPECIFICATIONS

### Absolute Maximum Ratings

DVSS = AVSSA = AVSSB = CVSS = 0V, DVDD = AVDDA = AVDDB

Parameter	Symbol	Rating	Unit
Supply voltage range	DVDD, AVDDA, AVDDB	-0.3 to 7.0	V
Input voltage range <sup>1</sup>	V <sub>IN</sub>	DVSS - 0.3 to DVDD + 0.3	V
Storage temperature range	T <sub>stg</sub>	-55 to 125	°C
Power dissipation	P <sub>D</sub>	250	mW

1. Pins DI, BCKI, WCKI, CKDVN, IWSL, RSTN, TSTN.

Also applicable during supply switching.

### Recommended Operating Conditions

DVSS = AVSSA = AVSSB = CVSS = 0V, DVDD = AVDDA = AVDDB

Parameter	Symbol	Rating	Unit
Supply voltage range	DVDD, AVDDA, AVDDB	4.5 to 5.5	V
Supply voltage variation	DVDD - AVDDA, DVDD - AVDDB, AVDDA - AVDDB, DVSS - AVSSA, DVSS - AVSSB, AVSSA - AVSSB, DVSS - CVSS, AVSSA - CVSS, AVSSB - CVSS	±0.1	V
Operating temperature range	T <sub>opr</sub>	-40 to 85	°C

## DC Electrical Characteristics

Recommended operating conditions, unless otherwise specified.

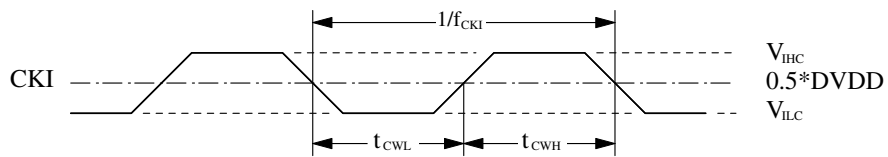
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DVDD, AVDDA, AVDDB supply current <sup>1</sup>	I <sub>DD</sub>	f <sub>CKI</sub> = 11.2896MHz	–	7	11	mA
		f <sub>CKI</sub> = 16.9344MHz	–	10	14	mA
		f <sub>CKI</sub> = 24.576MHz	–	15	19	mA
		f <sub>CKI</sub> = 36.864MHz	–	21	26	mA
CKI HIGH-level input voltage	V <sub>IHC</sub>		0.7 × DVDD	–	–	V
CKI LOW-level input voltage	V <sub>ILC</sub>		–	–	0.3 × DVDD	V
CKI input voltage	V <sub>INAC</sub>	AC coupling	1.0	–	–	Vp-p
HIGH-level input voltage <sup>2</sup>	V <sub>IH</sub>		2.4	–	–	V
LOW-level input voltage <sup>2</sup>	V <sub>IL</sub>		–	–	0.5	V
HIGH-level output voltage <sup>3</sup>	V <sub>OH</sub>	I <sub>OH</sub> = –1mA	DVDD – 0.4	–	–	V
LOW-level output voltage <sup>3</sup>	V <sub>OL</sub>	I <sub>OL</sub> = 1mA	–	–	0.4	V
CKI HIGH-level input current	I <sub>IHC</sub>	V <sub>IN</sub> = DVDD	30	60	120	μA
CKI LOW-level input current	I <sub>ILC</sub>	V <sub>IN</sub> = 0V	30	60	120	μA
LOW-level input current <sup>4</sup>	I <sub>IL2</sub>	V <sub>IN</sub> = 0V	–	5	15	μA
HIGH-level input leakage current <sup>5</sup>	I <sub>IH1</sub>	V <sub>IN</sub> = DVDD	–	–	1.0	μA
LOW-level input leakage current <sup>5</sup>	I <sub>IL1</sub>	V <sub>IN</sub> = 0V	–	–	1.0	μA
HIGH-level input leakage current <sup>4</sup>	I <sub>IH2</sub>	V <sub>IN</sub> = DVDD	–	–	1.0	μA

1. No output load, NPC-standard input data pattern.
2. Pins DI, BCKI, WCKI, CKDVN, IWSL, RSTN, TSTN.
3. Pin TO.
4. Pins CKDVN, IWSL, RSTN, TSTN.
5. Pins DI, BCKI, WCKI.

## AC Electrical Characteristics

### System clock Input (CKI)

Parameter	Symbol	Rating			Unit
		min	typ	max	
CKI clock frequency	$f_{CKI}$	5	–	60	MHz
HIGH-level clock pulsewidth	$t_{CWH}$	5	–	–	ns
LOW-level clock pulsewidth	$t_{CWL}$	5	–	–	ns



### Internal System Clock

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Internal system clock frequency	$f_{SYS}$		5	–	46	MHz

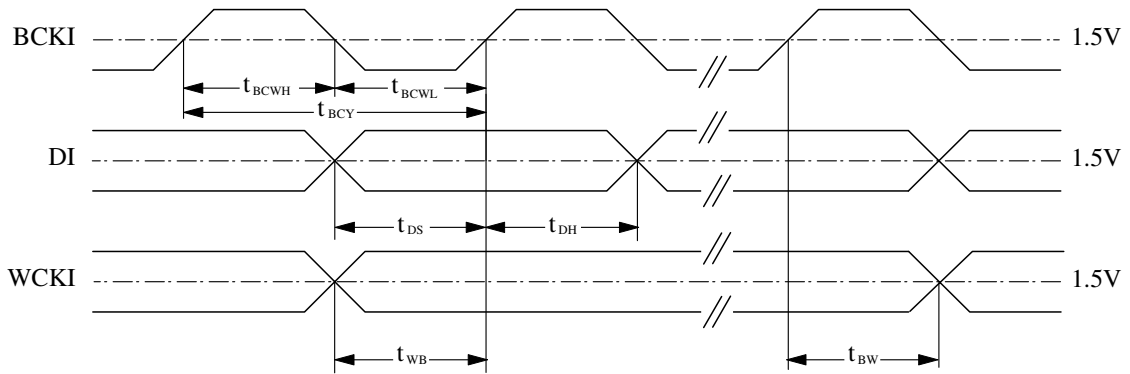
Internal system clock frequency is the same as the CKI clock frequency when CKDVN = HIGH.  
Internal system clock frequency is half the CKI clock frequency when CKDVN = LOW.

### Reset Input (RSTN)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
RSTN LOW-level pulsewidth	$t_{RSTN}$	At power ON	1	–	–	$\mu$ s
		After power ON	100	–	–	ns

**Serial input (BCKI, DI, WCKI)**

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	$t_{BCWH}$	10	–	–	ns
BCKI LOW-level pulsewidth	$t_{BCWL}$	10	–	–	ns
BCKI pulse cycle	$t_{BCY}$	22	–	–	ns
DI setup time	$t_{DS}$	5	–	–	ns
DI hold time	$t_{DH}$	5	–	–	ns
WCKI edge to first BCKI rising edge	$t_{WB}$	10	–	–	ns
Last BCKI rising edge to WCKI edge	$t_{BW}$	10	–	–	ns



**Group Delay**

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Group delay <sup>1</sup>	$T_{gd}$		–	–	2/fsi	s

1. fsi is the input sampling rate of SM5865CM.

For example, fsi is 384kHz when this LSI is used in combination with an 8-times oversampling digital filter of which input sampling rate is 48kHz.

## AC Analog Characteristics

### Measurement Conditions

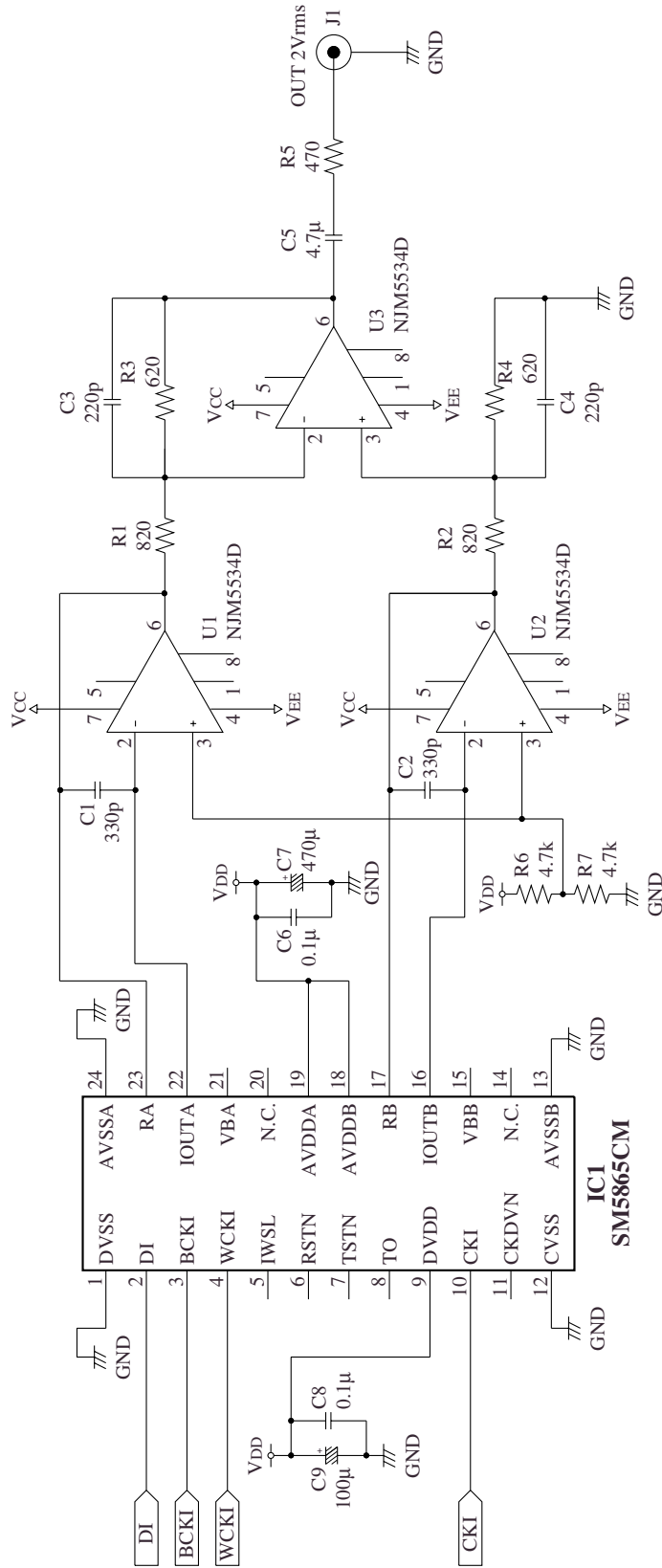
External 8fs digital filter	:	NPC SM5847AF
External operational amplifier	:	JRC NJM5534D
Supply voltage SM5865CM	:	DVDD = AVDDA = AVDDB = 5V, DVSS = AVSSA = AVSSB = CVSS = 0V
SM5847AF	:	+ 3.3V
NJM5534D	:	± 15V
Ambient temperature	:	25°C
Input data of SM5847AF	:	48kHz sampling (fs), 24-bit data
System clock	:	24.576MHz (= 512fs), (64fs noise shaper operation)
Audio analyzer	:	Audio Precision System Two (RMS mode)
Measurement filter condition	:	THD + N 22HzHPF, 20kHzLPF (FLP-A20K)
	:	D.R 22HzHPF, 22kHzLPF, A-weight (FIL-AWT)
	:	S/N 22HzHPF, 22kHzLPF, A-weight (FIL-AWT)
Measurement circuits diagram	:	See next page.

### Analog Characteristics

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output level <sup>1</sup>	$V_{out}$	1kHz, 0dB	1.28	1.33	1.38	Vrms
Total harmonic distortion	THD + N	1kHz, 0dB	-	0.00030 (- 110.5dB)	0.00060 (- 104.4dB)	%
Dynamic range	D.R	1kHz, -60dB	111	117	-	dB
Signal-to-noise ratio	S/N	1kHz, 0/-∞dB	117	120	-	dB
Gain drift	G.D		-	10	-	ppm/°C

1.  $V_{out}$  is the output level of the first I-V conversion stage.

Measurement circuit



Dynamics Characteristics (under Measurement Conditions in page 8)

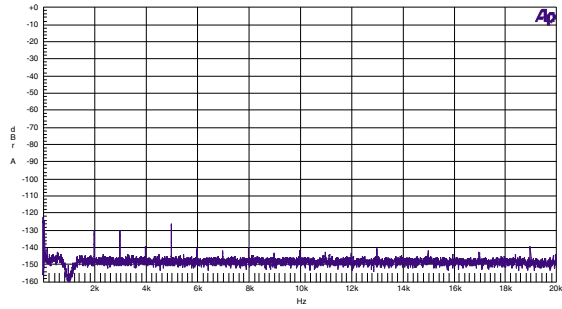


Figure 1. 0dB input FFT (1)  
(1kHz notchfilter 32768point 8average)

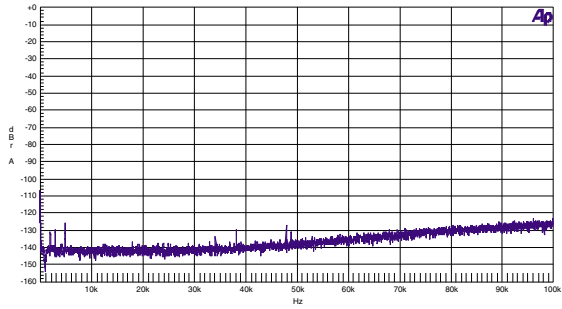


Figure 2. 0dB input FFT (2)  
(1kHz notchfilter 32768point 8average)

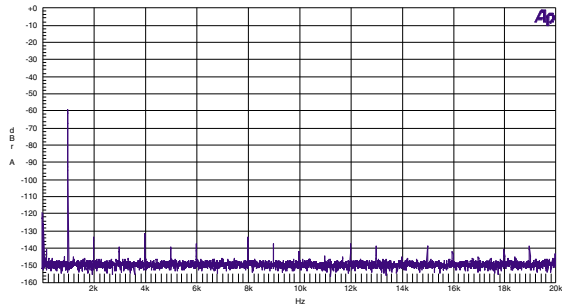


Figure 3. -60dB input FFT (32768point 8average)

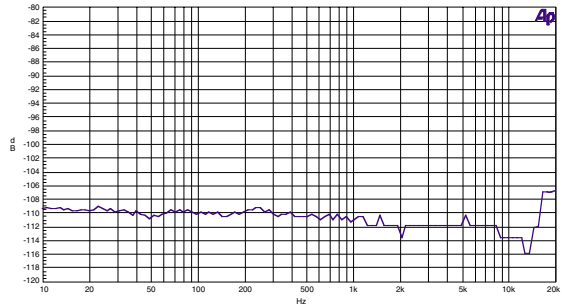


Figure 4. THD + N vs. Frequency

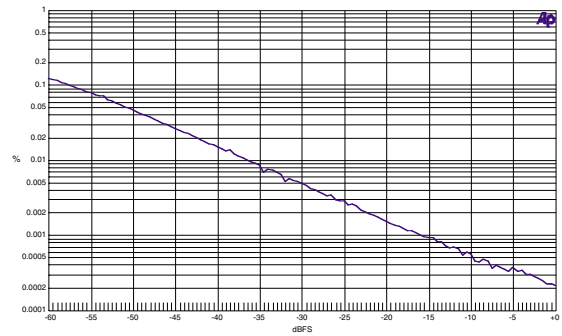


Figure 5. THD + N(%) vs. Amplitude

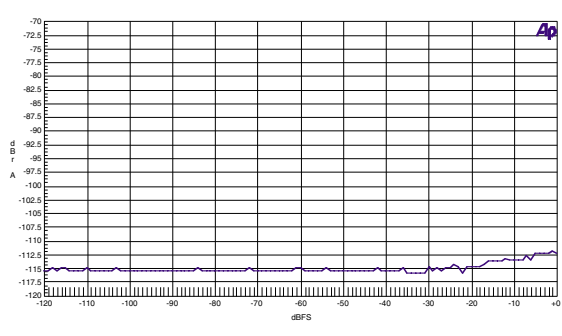


Figure 6. THD + N (dB) vs. Amplitude

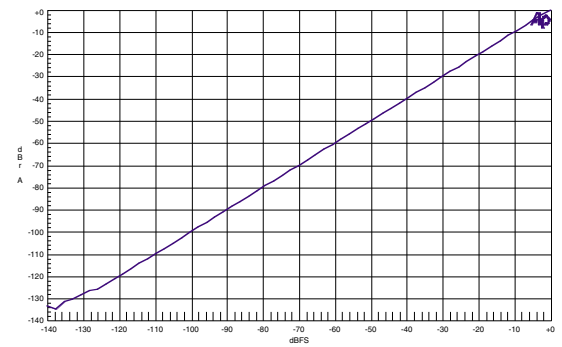


Figure 7. Linearity

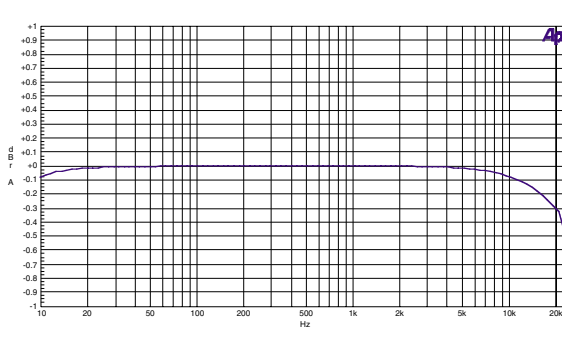


Figure 8. Evaluation Board Frequency Response

## FUNCTIONAL DESCRIPTION

### Analog Outputs

#### IOUTA, IOUTB

The SM5865CM input data in-phase signal is processed by noise shaper A and 31-level DEM-DAC with current output on differential output A, and input data reverse-phase signal is processed by noise shaper B and 31-level DEM-DAC with current output on differential output B. Differential outputs A and B also have separate in-phase and reverse-phase outputs: A in-phase output and B reverse-phase output are connected internally and output on IOUTA, and B in-phase output and A reverse-phase output are connected internally and output on IOUTB.

The IOUTA and IOUTB current outputs are I/V converted by external circuit and then input to a differential input op-amp to obtain the final analog signal.

#### RA, RB

Internal resistors are connected between IOUTA and RA pins and between IOUTB and RB pins, which serve as the op-amp feedback resistors. The feedback resistors have a resistance of 4.7k $\Omega$ .

The I/V converter output gain can be adjusted by connecting external resistors in parallel or serial with the internal resistors. Note, however, that the internal resistance can vary from device to device by  $\pm 10\%$ , and if external resistors are used, the output level changes depending on the difference between each resistor ratio. If the I/V converter gain is increased, a dynamic range higher even than that given in “Analog Characteristics (page 8)” can be obtained.

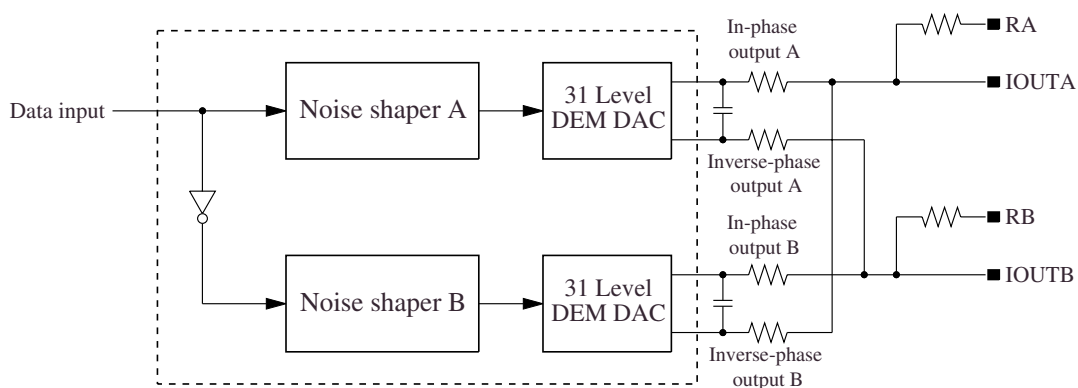


Figure 9. Analog outputs

## VBA, VBB

A 0.5VDD signal is output from VBA, VBB using a resistor divider network. Using these pins allows the use of the SM5865CM to replace the pin-compatible SM5865BM product.

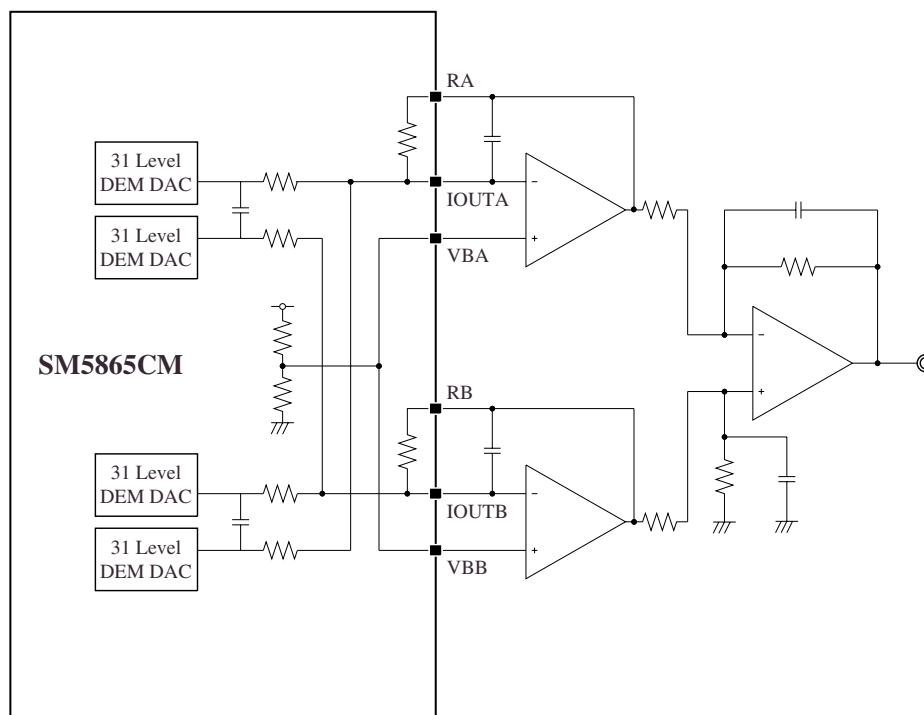


Figure 10. VBA, VBB

## Audio Data Input (DI, BCKI, WCKI, IWSL)

### ■ Input data format

The audio data is input in MSB-first, 2s-complement, 24-bit/20-bit serial format. The input word bit length is selected by IWSL, 24-bit when HIGH, and 20-bit when LOW.

### ■ Jitter-free function

The SM5865CM serial input data from DI synchronize with the word clock (WCKI) and are read into the first register stage, and those also synchronize with the clock derived from divided system clock and are read into the next register stage. This word clock and the system clock are always phase compared. When a phase shift was detected, the comparison result is used to perform input timing adjustment in the system clock. Therefore this process enable internal calculations not to be affected by generated large jitter on the word clock or changing the sampling rate during inputting data.

## System Clock Divider (CKDVN)

The SM5865CM has a built-in clock frequency divider. The divider enables the internal system clock to operate at half the input frequency, for example when the external system clock input frequency is high.

## System Reset (RSTN)

The device should be reset in the following cases.

- At power ON
- When the system clock CKI stops, or other abnormalities occur.

The device is reset by applying a LOW-level pulse on RSTN.

## Theoretical Quantization Noise Reduction

The SM5865CM employs a 3rd-order 31-level quantized noise shaper to widely reduce quantization noise in the audio band to the high frequency bandwidth. The theoretical quantization noise level at 16fs to 96fs operation is shown in figure 11.

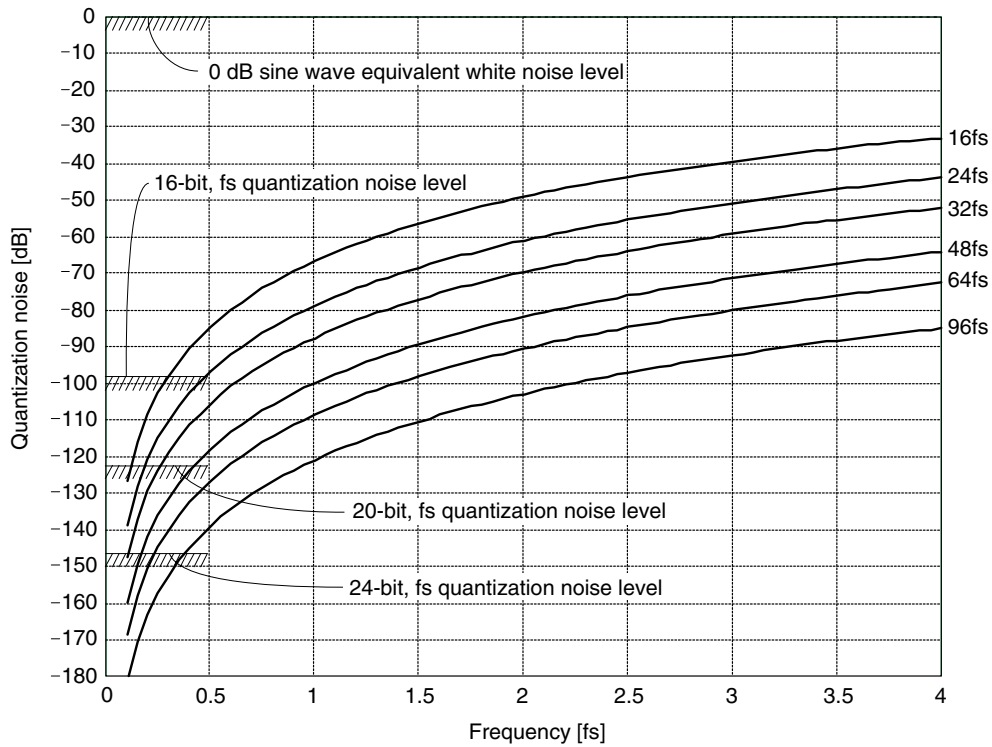


Figure 11. Theoretical quantization noise level

### Internal Oversampling Operation

The SM5865CM accepts data output from an 8-times or 4-times oversampling digital filter, and oversampled internally again up to the noise shaper operating rate. The internal oversampling factor is determined automatically from the system clock input frequency and the input sampling frequency. This internal oversampling factor (n) must be an integer satisfying the conditions shown in table 1.

Table 1. Operating conditions

Parameter	CKDVN = HIGH	CKDVN = LOW
$f_{WCKI}$ and $f_{CKI}$ compulsory conditions <sup>1</sup>	$f_{CKI} = f_{WCKI} \times 8 \times n$ where n = 1, 2, 3, ...	$f_{CKI} = f_{WCKI} \times 16 \times n$ where n = 1, 2, 3, ...
Noise shaper operating frequency	$f_{ns} = f_{WCKI} \times n = \frac{f_{CKI}}{8}$	$f_{ns} = f_{WCKI} \times n = \frac{f_{CKI}}{16}$

1.  $f_{WCKI}$  = word clock frequency,  $f_{CKI}$  = input system clock frequency, n = internal oversampling factor

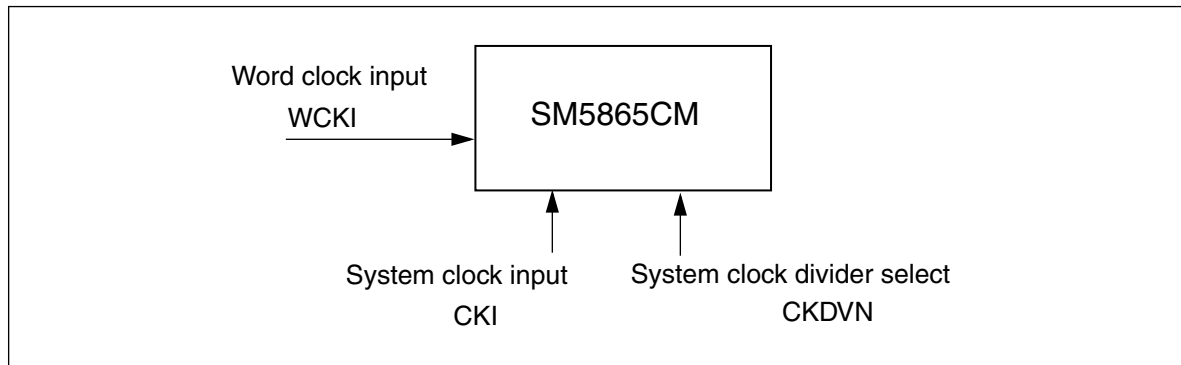


Figure 12. Clock-related inputs

## System Clock Frequencies

Table 2 shows some possible combinations for the circuit configuration shown in figure 13.

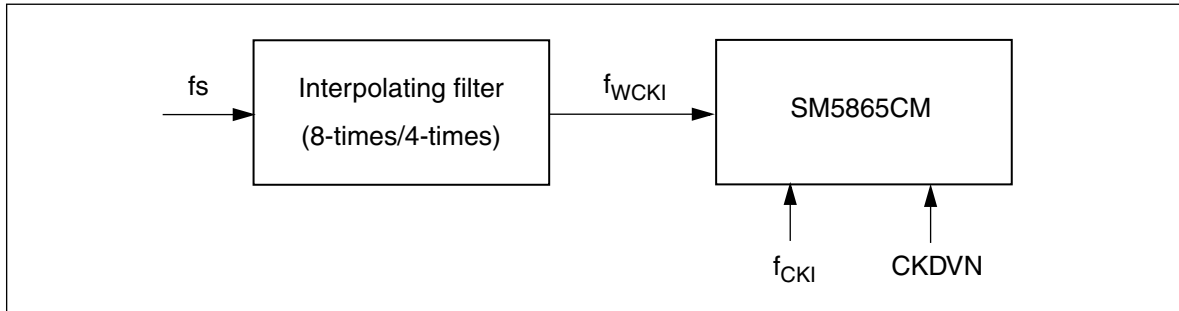


Figure 13. Circuit configuration

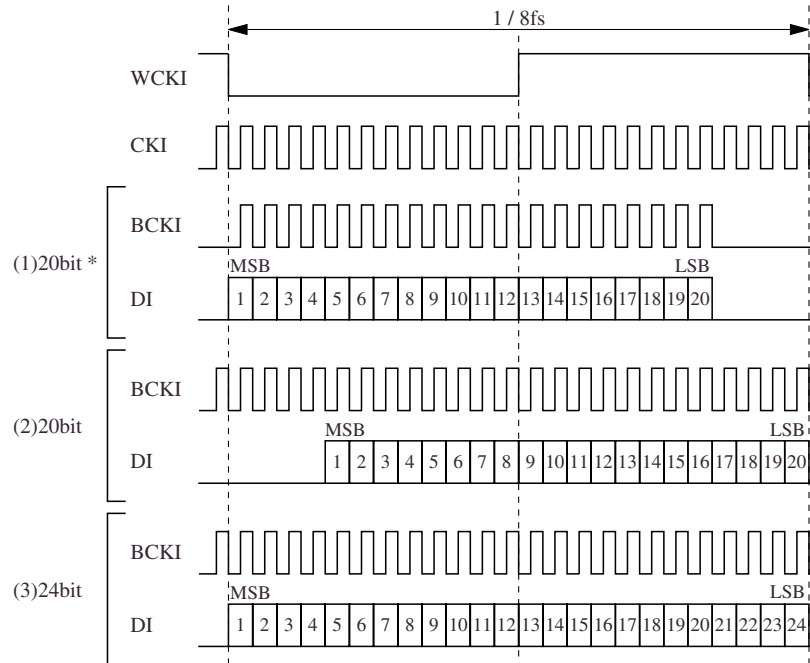
Table 2. System clock frequencies (CKDVN = HIGH)

fs	System clock frequency <sup>1</sup> f <sub>CK1</sub>	Noise shaper operating rate	Internal factor (8fs input)	Internal factor (4fs input)
16kHz	6.144MHz (384fs)	48fs	6	12
16kHz	8.192MHz (512fs)	64fs	8	16
16kHz	12.288MHz (768fs)	96fs	12	24
32kHz	6.144MHz (192fs)	24fs	3	6
32kHz	8.192MHz (256fs)	32fs	4	8
32kHz	12.288MHz (384fs)	48fs	6	12
32kHz	16.384MHz (512fs)	64fs	8	16
32kHz	24.576MHz (768fs)	96fs	12	24
44.1kHz	8.4672MHz (192fs)	24fs	3	6
44.1kHz	11.2896MHz (256fs)	32fs	4	8
44.1kHz	16.9344MHz (384fs)	48fs	6	12
44.1kHz	22.5792MHz (512fs)	64fs	8	16
44.1kHz	33.8688MHz (768fs)	96fs	12	24
48kHz	9.216MHz (192fs)	24fs	3	6
48kHz	12.288MHz (256fs)	32fs	4	8
48kHz	18.432MHz (384fs)	48fs	6	12
48kHz	24.576MHz (512fs)	64fs	8	16
48kHz	36.864MHz (768fs)	96fs	12	24
88.2kHz	16.9344MHz (192fs)	24fs	3	6
88.2kHz	22.5792MHz (256fs)	32fs	4	8
88.2kHz	33.8688MHz (384fs)	48fs	6	12
88.2kHz	45.1584MHz (512fs)	64fs	8	16
96kHz	18.432MHz (192fs)	24fs	3	6
96kHz	24.576MHz (256fs)	32fs	4	8
96kHz	36.864MHz (384fs)	48fs	6	12
176.4kHz	33.8688MHz (192fs)	24fs	3	6
176.4kHz	45.1584MHz (256fs)	32fs	4	8
192kHz	36.864MHz (192fs)	24fs	3	6

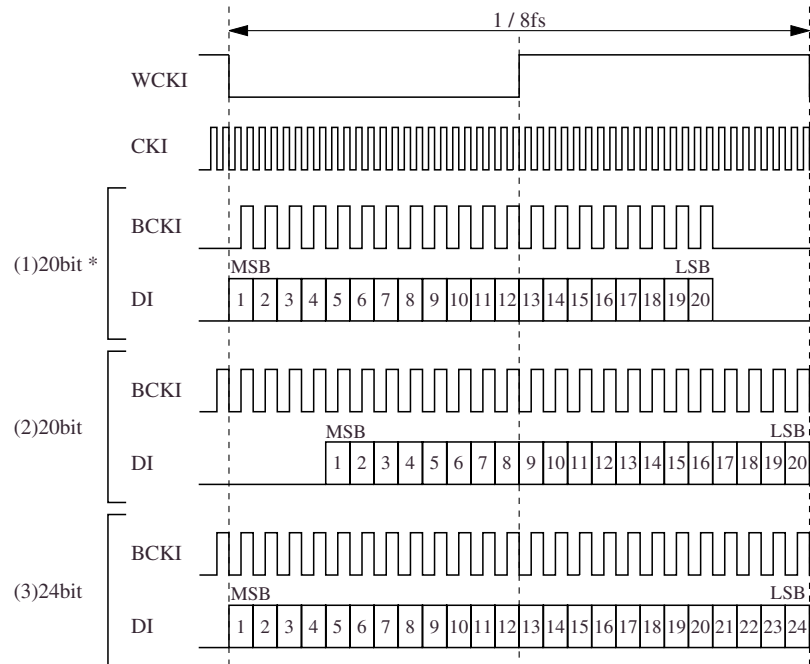
1. When CKDVN = LOW, the system clock frequency f<sub>CK1</sub> is halved, so the values shown are half the input frequency required for the same sampling rate and internal factors.

## TIMING DIAGRAMS

### 192fs System Clock Input Timing

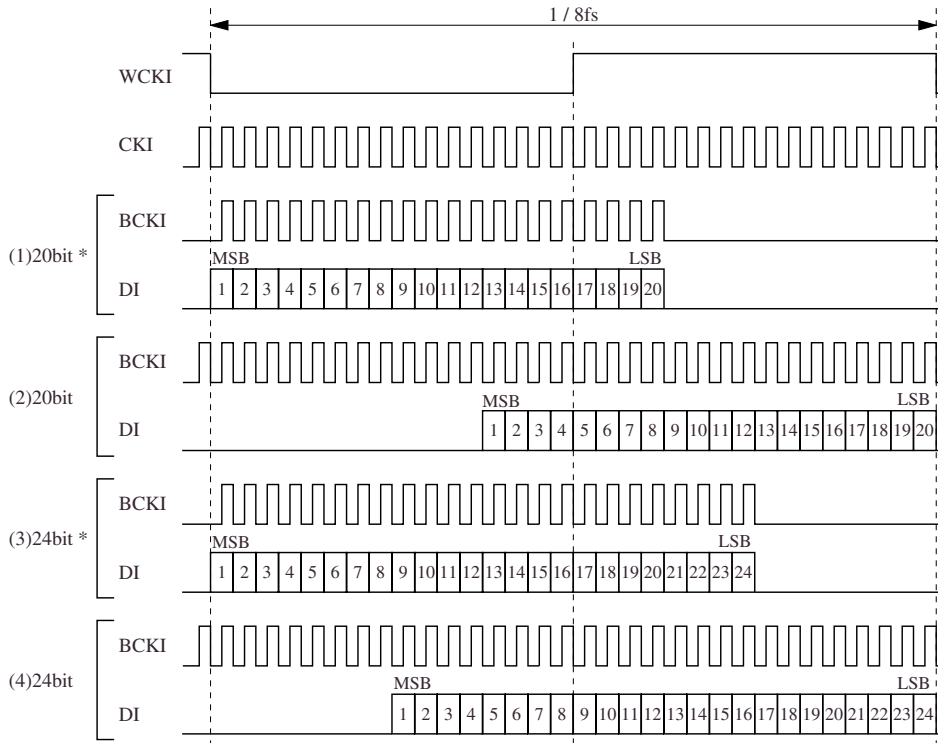


### 384fs System Clock Input Timing

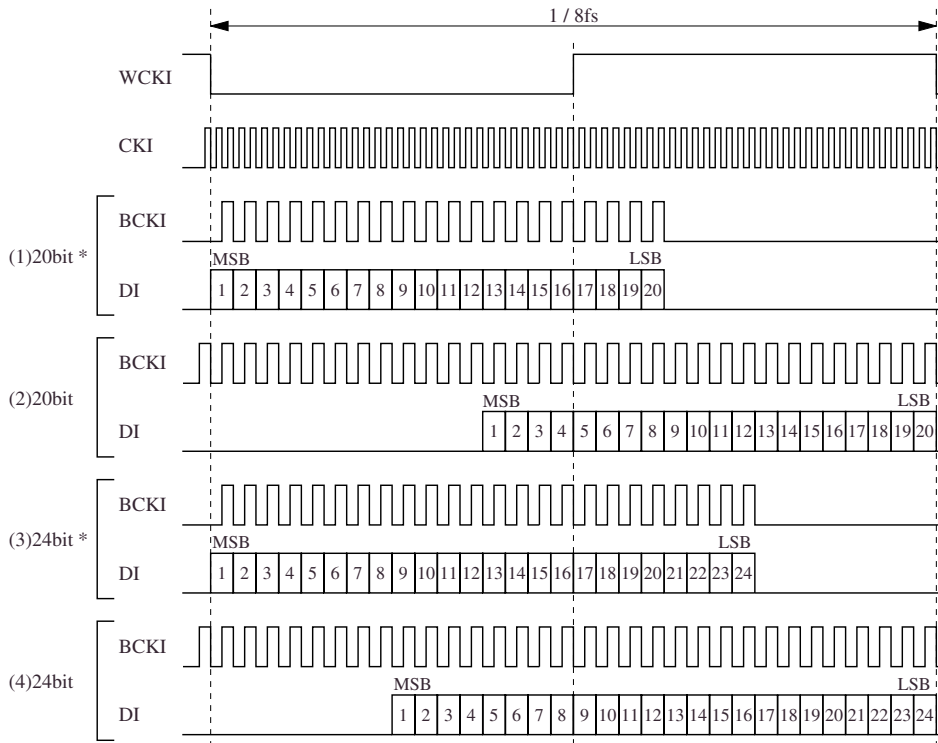


\*: Data can be input at any period within the word clock cycle.

256fs System Clock Input Timing



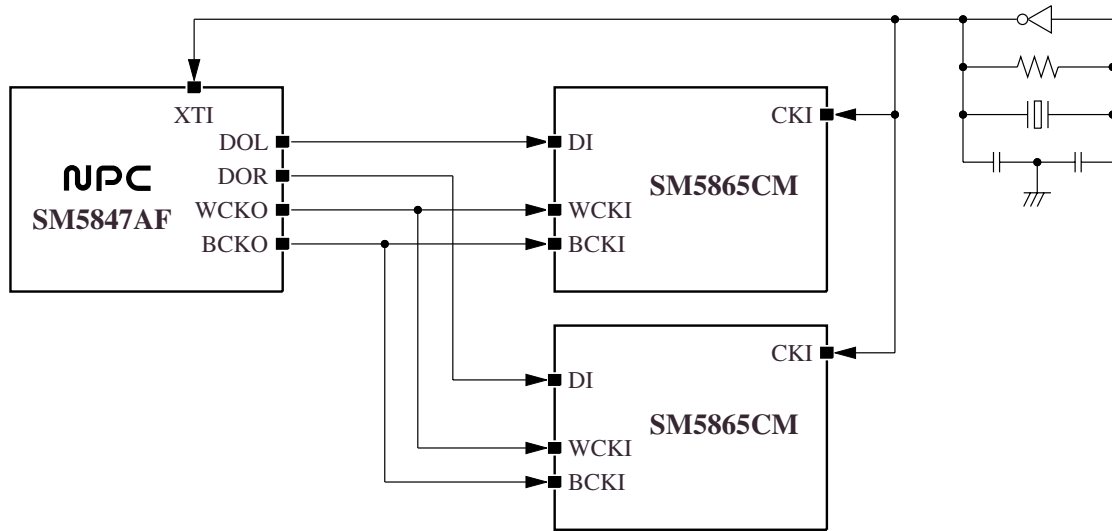
512fs System Clock Input Timing



\*: Data can be input at any period within the word clock cycle.

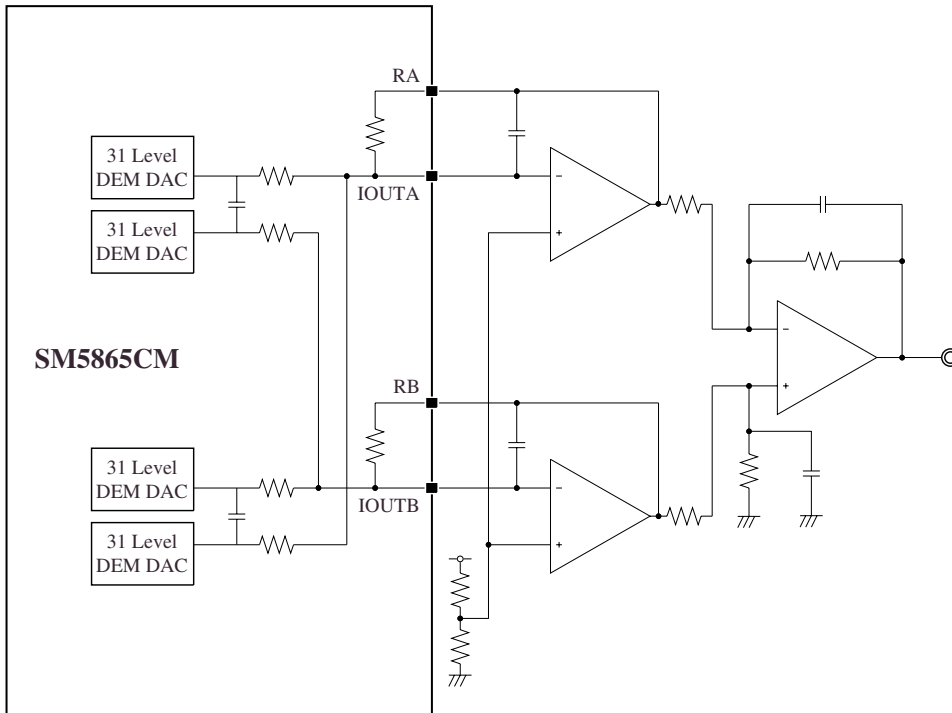
TYPICAL APPLICATIONS

Input Interface Circuit

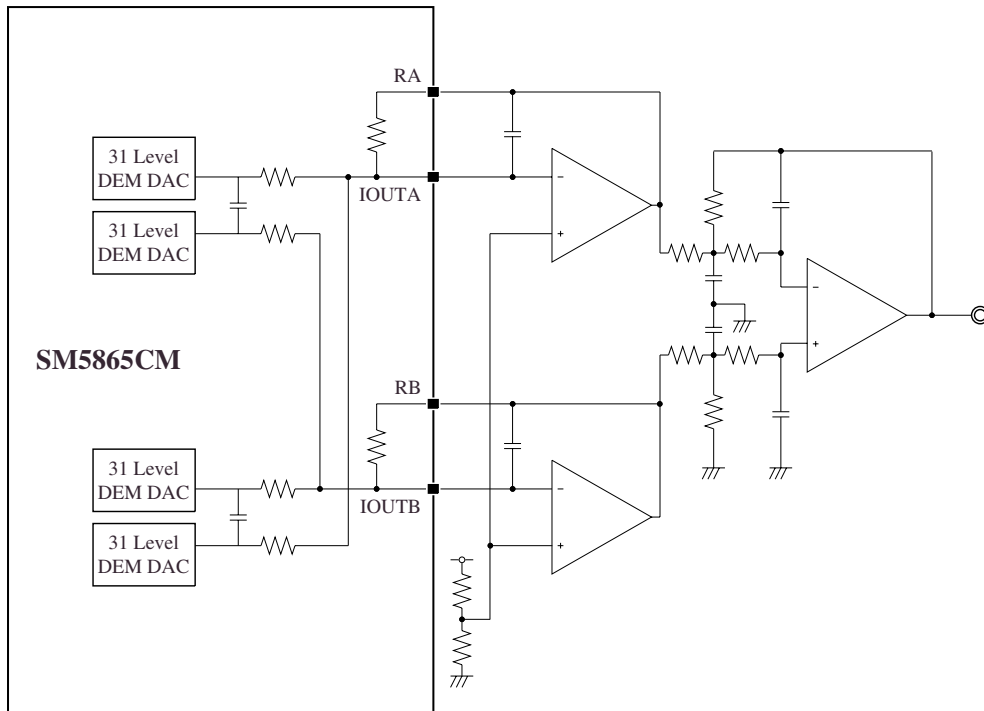


Analog Output Circuits

Analog Output Circuit 1



Analog Output Circuit 2



Note that the output analog characteristics and other specifications are not guaranteed for particular formats or application circuits.  
 Note that NPC has no responsibility for patents related to application circuits in these datasheets.

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